集成电路版图设计技术

Layout Techniques of the Integrated Circuit

聂凯明

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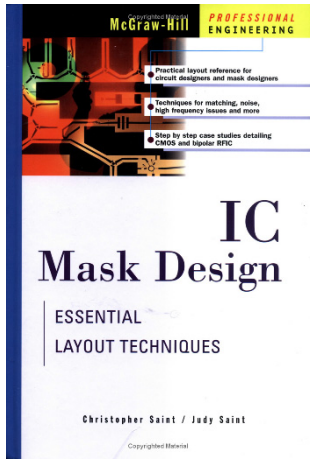
Lecture 1:

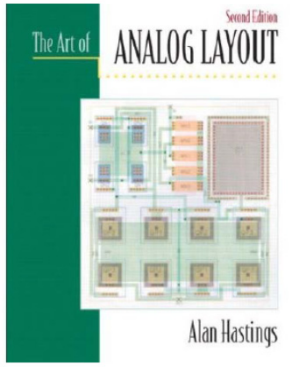
Basic Knowledge of Layout Techniques

Info. Of the Class



Reference Book:

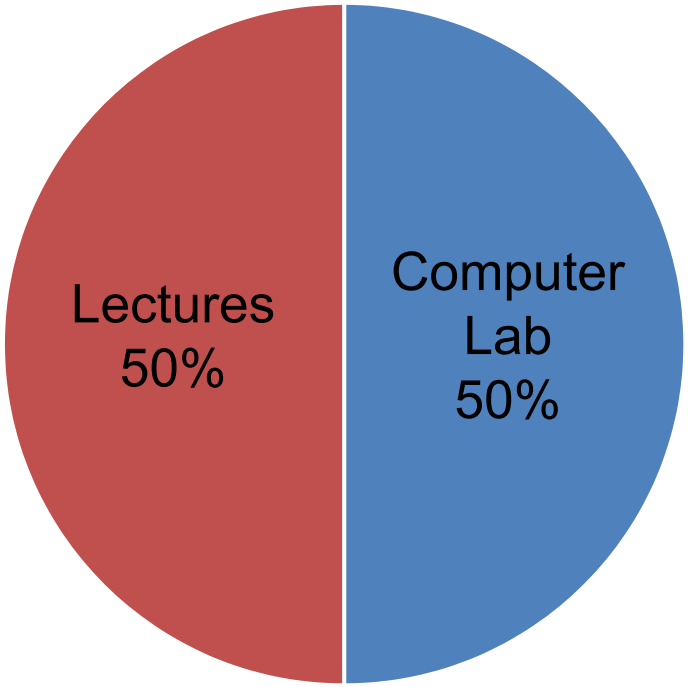
Christopher Saint, Judy Saint, IC Mask Design: Essential Layout Techniques,1st, McGraw-Hill Professional, 2004.

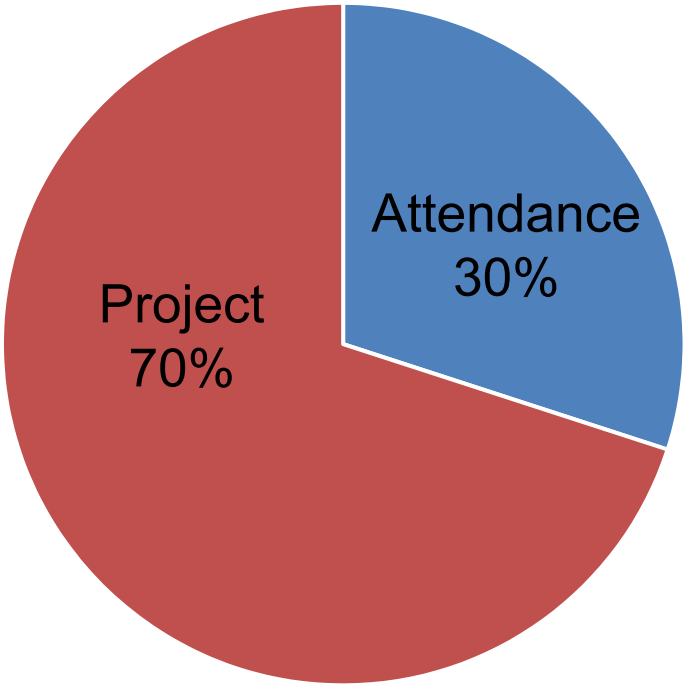


Selective Reading:

Alan Hastings, The Art of Analog Layout, 2nd, Prentice Hall, 2005.

Info. Of the Class





Introduction

The layout of an IC defines the geometry of the masks used in fabrication (multi-layer drawing)

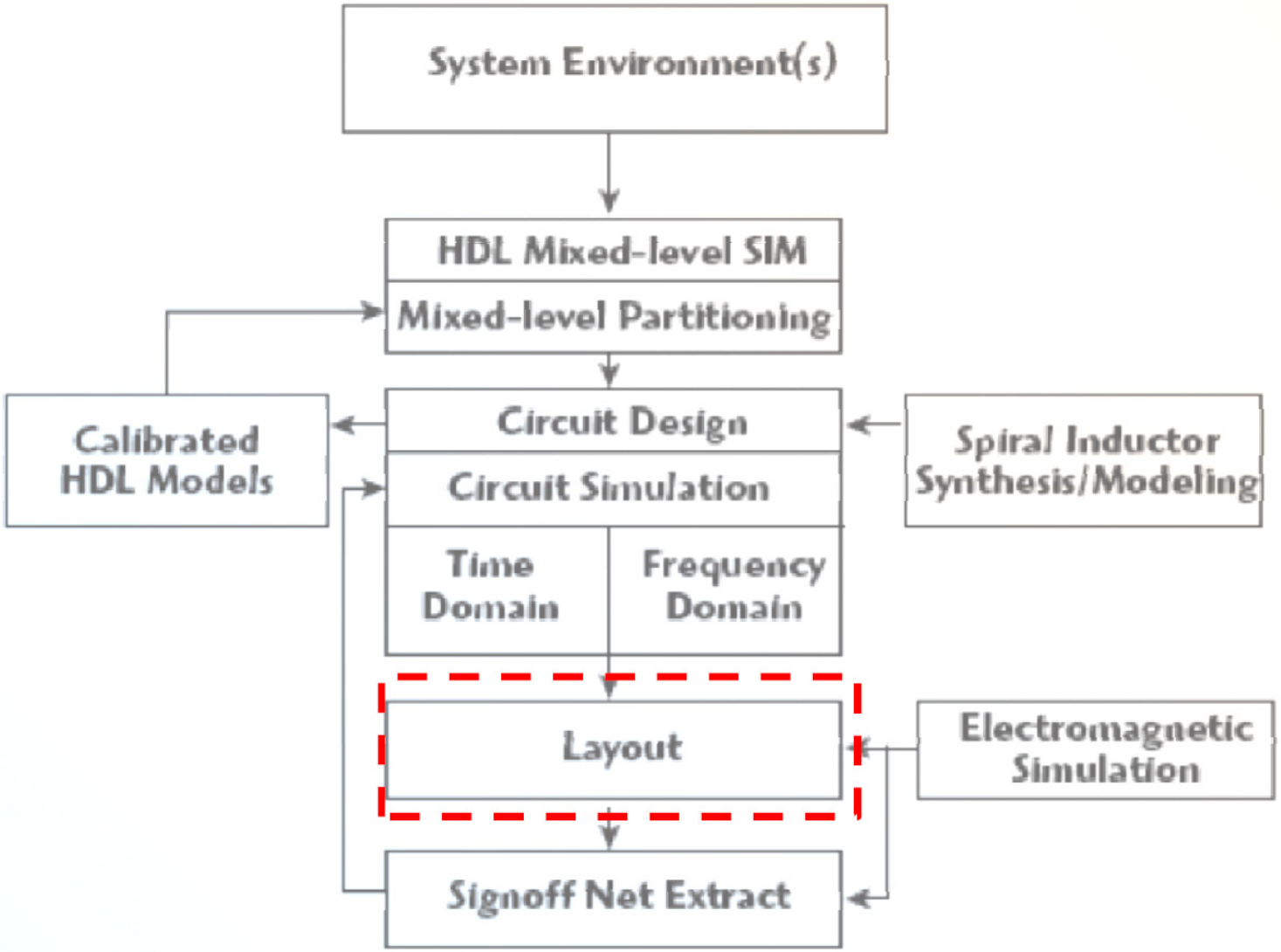
- Layout must conform the design rules of the technology used
- The layout of a digital circuit mainly affect speed performances
  - minimize and match delays
  - minimize the chip area
- The layout of an analog circuit may affect speed and precision
  - respect symmetries
  - match components
  - minimize parasitic
  - minimize offset
  - avoid interference
  - optimize interconnections
  - make an artistic work

Introduction

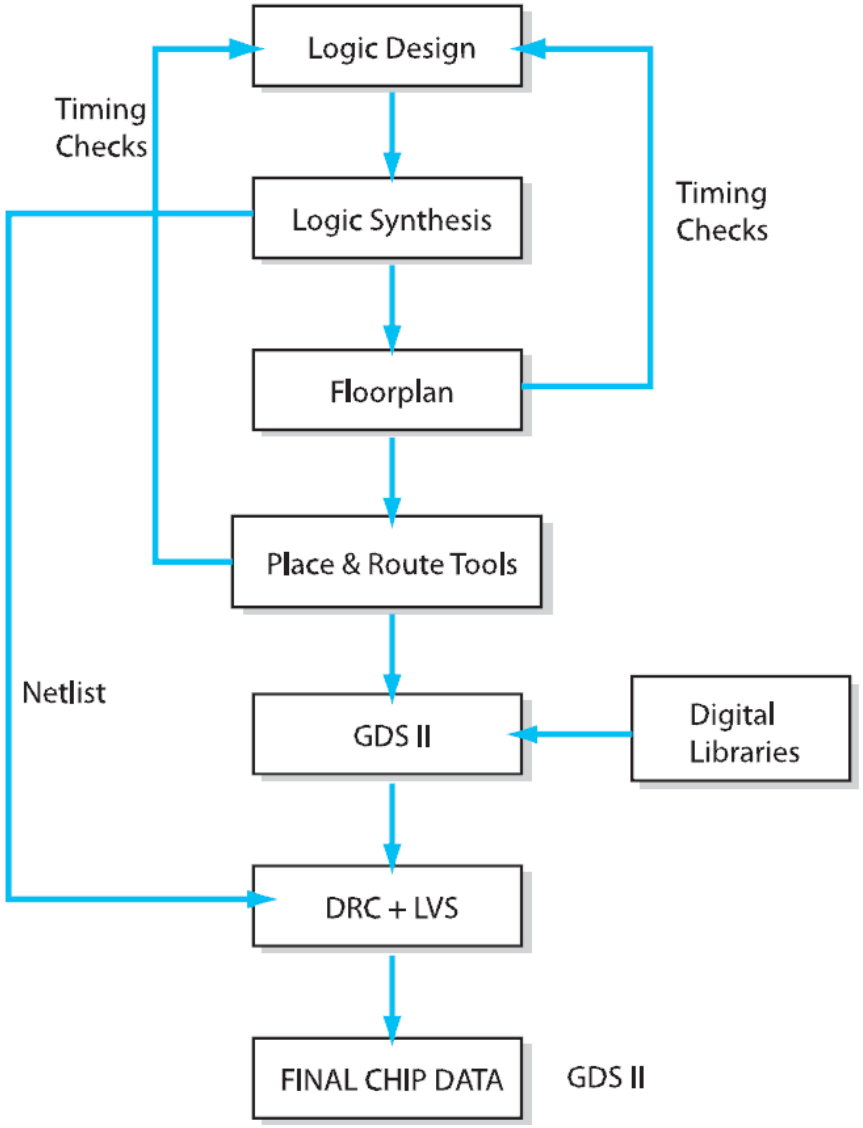
- Layout requires basic knowledge in IC technology
- Layout requires some knowledge in circuit design
- Analog Layout requires patience and style

- Layout is not drawing but planning!
  - have in mind what you want to do before starting
  - have a complete picture of the design
  - have “analog mindsets” and strictly follow them

Analog Integrated Circuit Design Flow

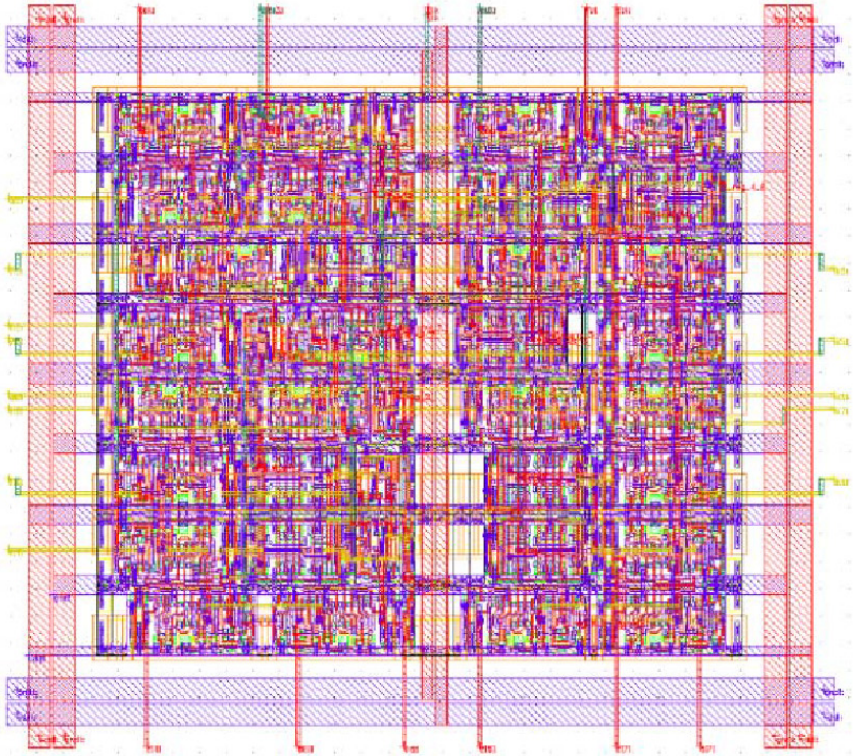


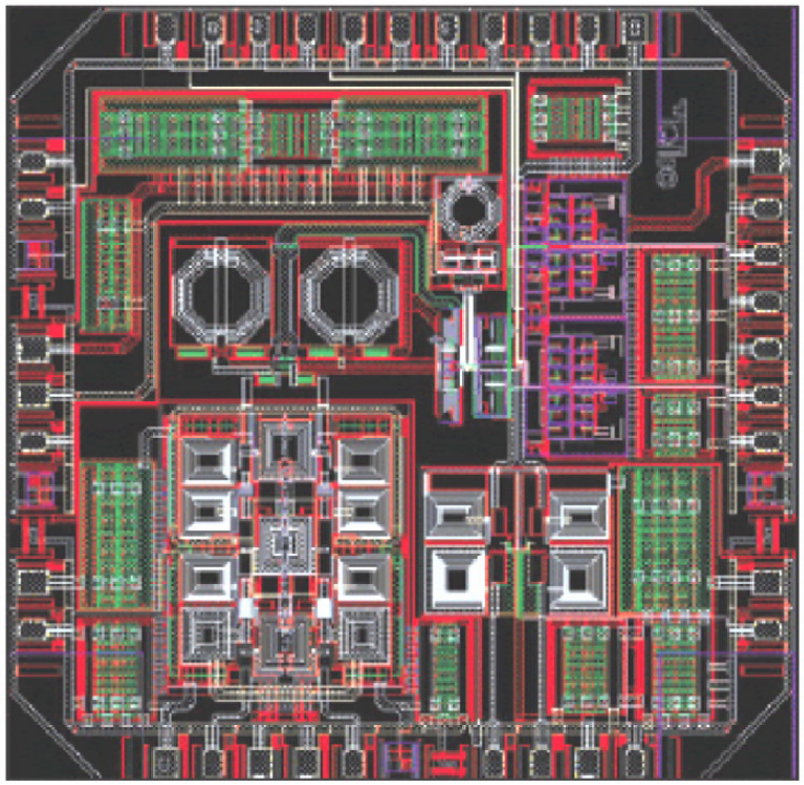
Digital Design Flow



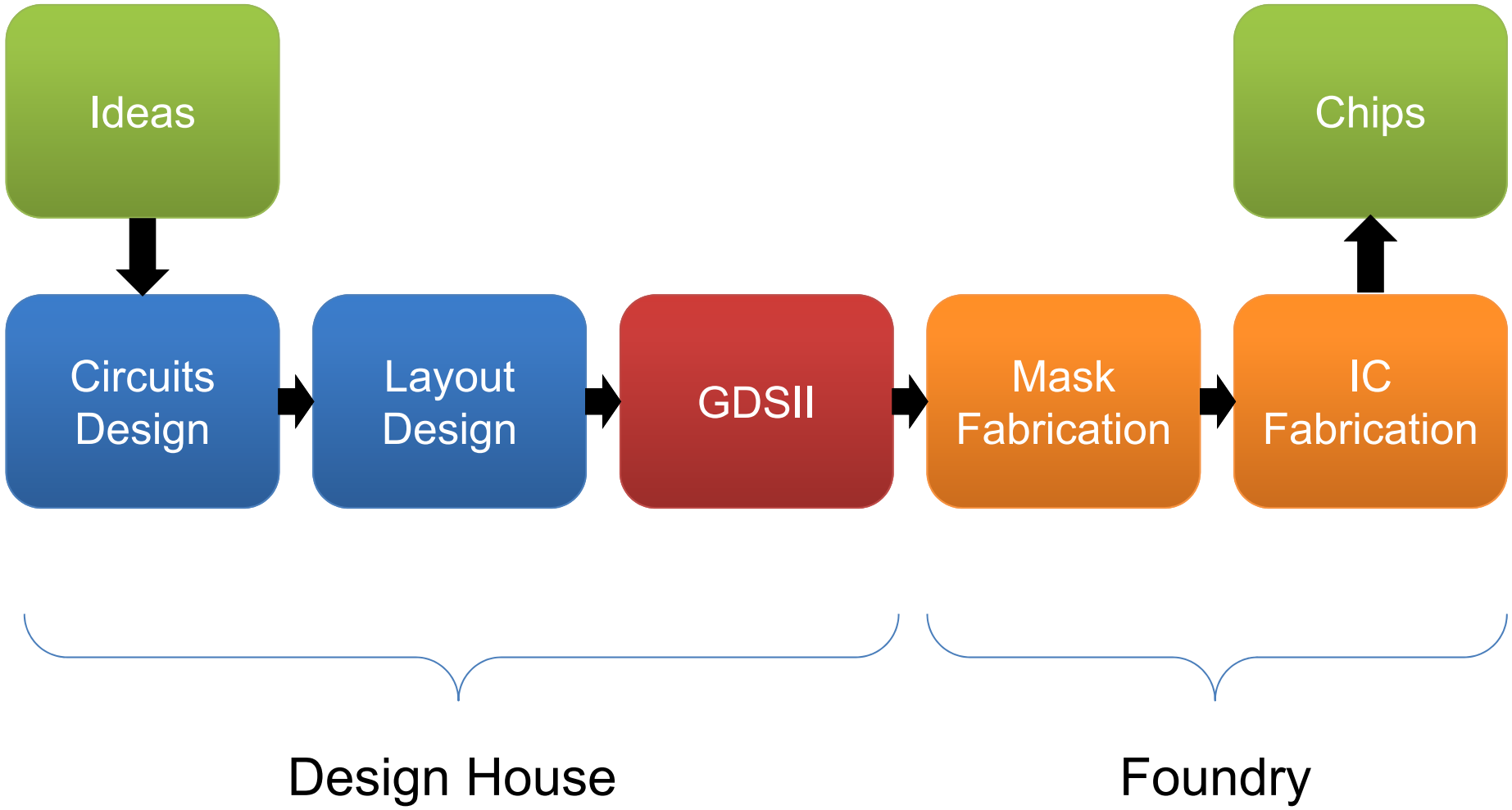
Monolithic Layout

Analog IC V.S. Digital IC



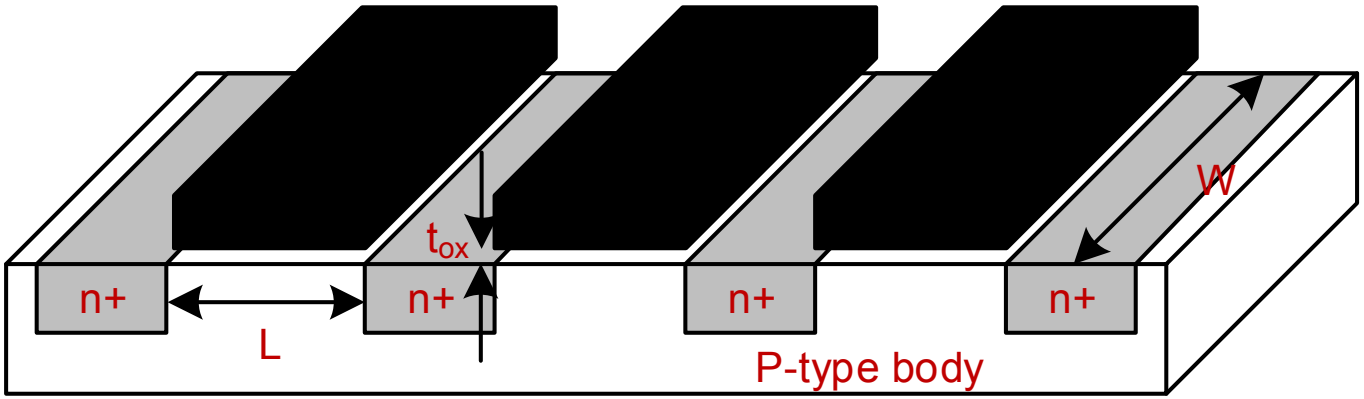


Tapeout Flow

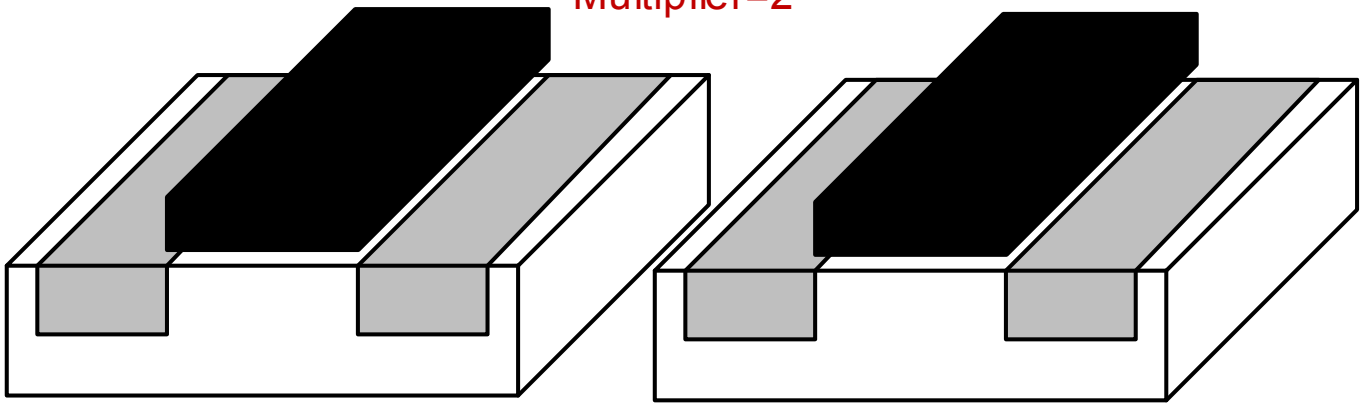


CMOS Transistor Parameters

Finger=3

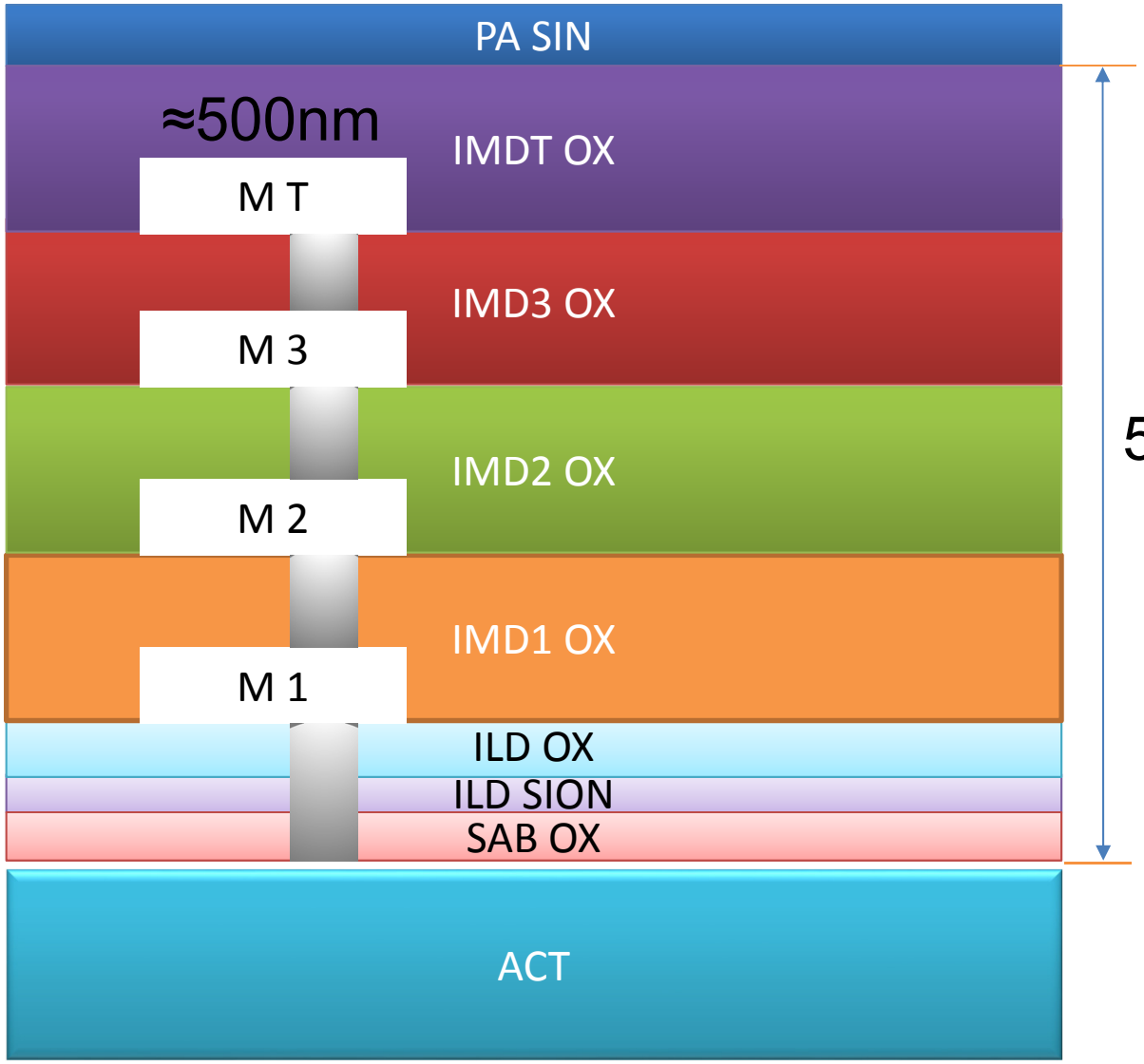


Multiplier=2



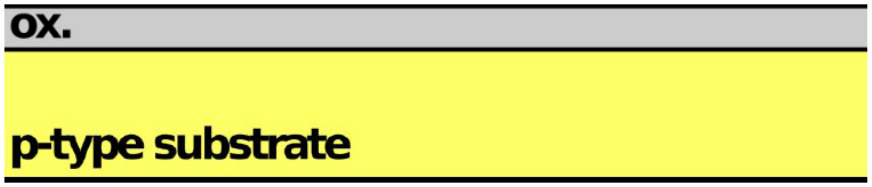
Total W/L=W/L × finger × multiplier

Semiconductor Process

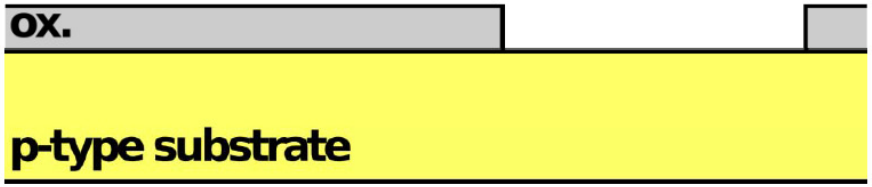


Process Flow

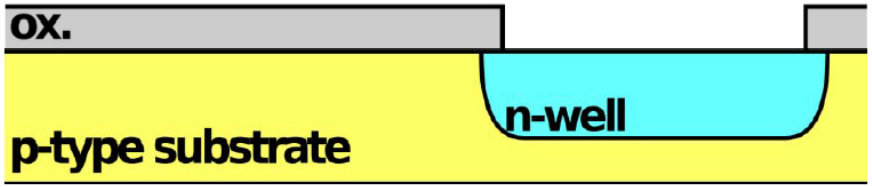
1. Grow field oxide



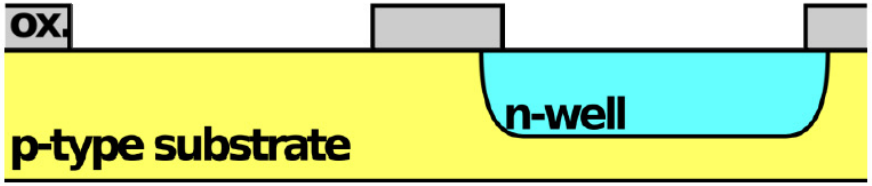
2. Etch oxide for pMOSFET



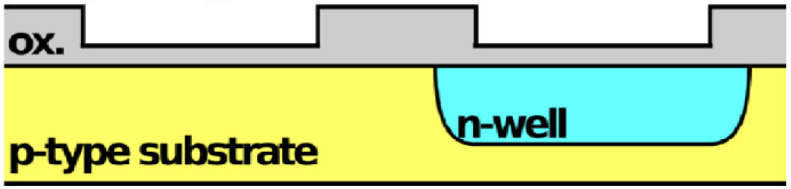
3. Diffuse n-well



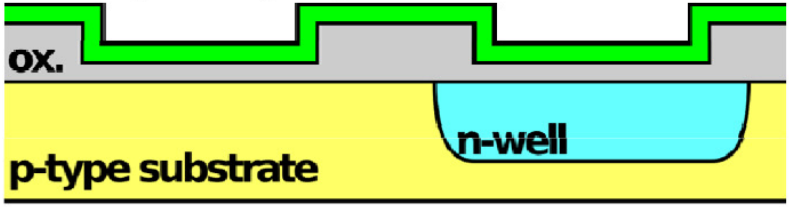
4. Etch oxide for nMOSFET



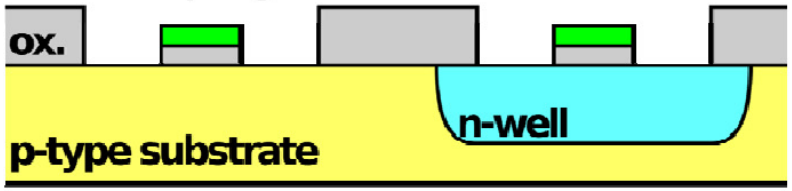
5. Grow gate oxide



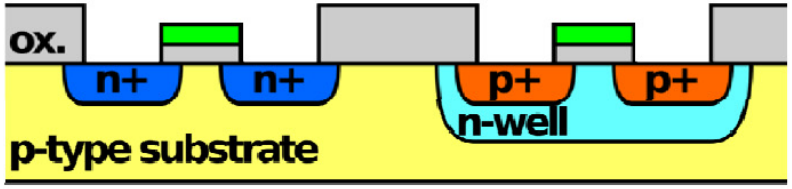
6. Deposit polysilicon



7. Etch polysilicon and oxide

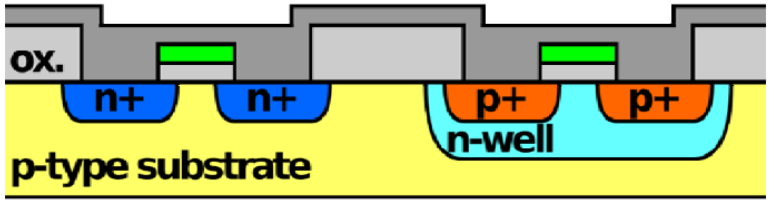


8. Implant sources and drains

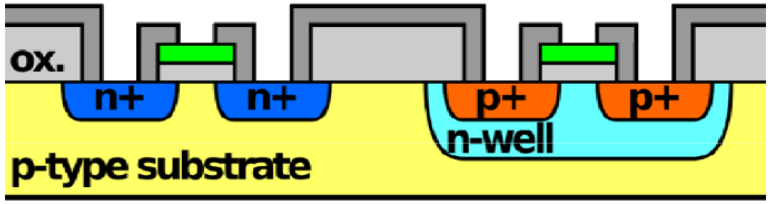


Process Flow

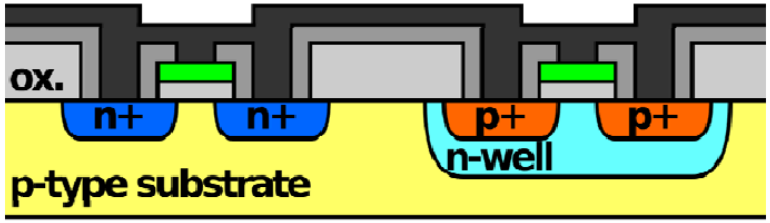
9. Grow nitride



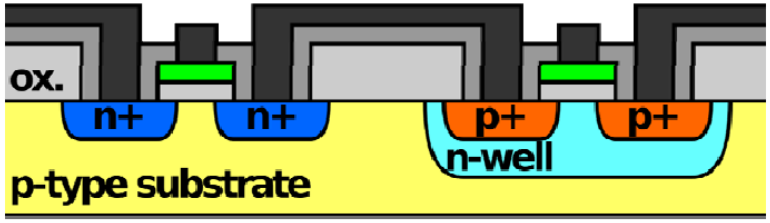
10. Etch nitride



11. Deposit metal

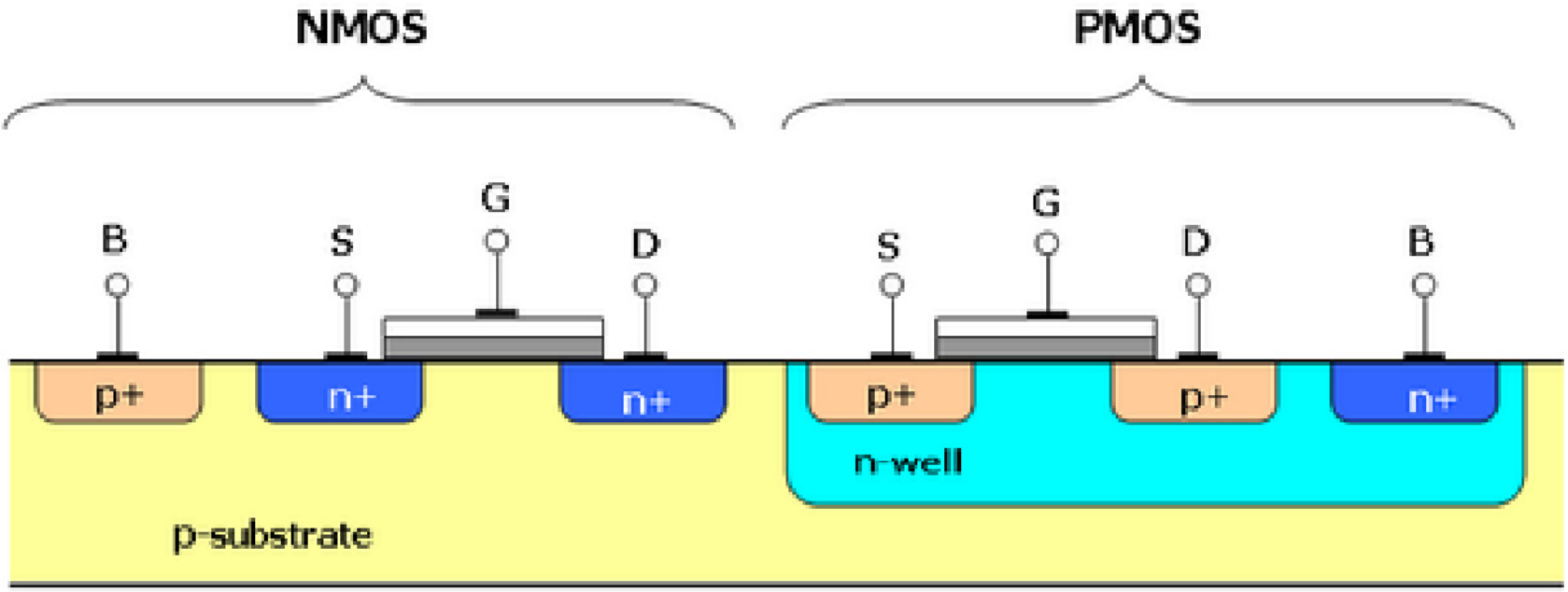


12. Etch metal



CMOS Transistors

Cross Section



Design Rule Terminologies

Definition	Symbol	Sample	Note	Fig.
Width	w	Width	w is used for line width	1
	l	Length and channel length	l is used for line length and channel length of MOSFET.	
Size	s	A size	s is used for square hole (e.g. Contact, metal Via)	2
spacing	d	Spacing of A to A	distance between two exclusive objects in the same layer	3
		Spacing of A to B	distance between two exclusive objects in different layers	4
enclosure	m	Enclosure of A beyond B	edge to edge distance between two inclusion objects (A encloses B)	5
extension	m	Extension of A beyond B (m1) , Extension of B beyond A (m2)	edge to edge external distance when one object extends beyond another	6
overlap	m	Overlap of A and B	edge to edge internal space when one object overlaps to another	7

Design Rule Terminologies

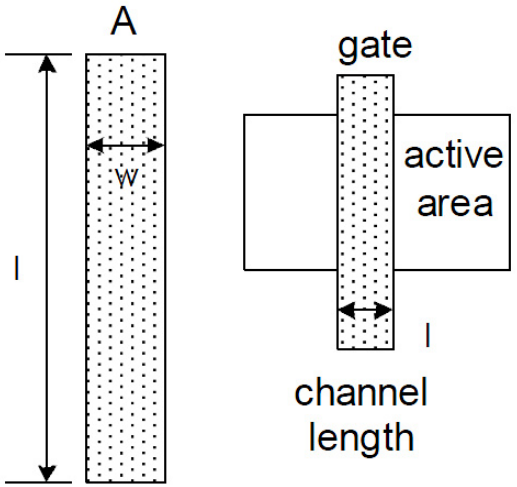


Fig 1

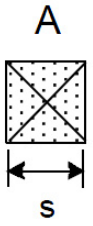


Fig 2

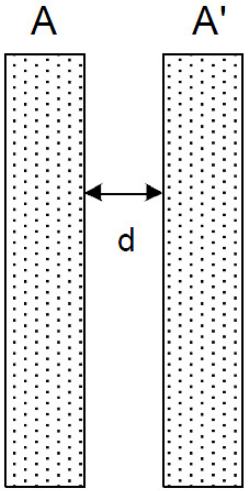


Fig 3

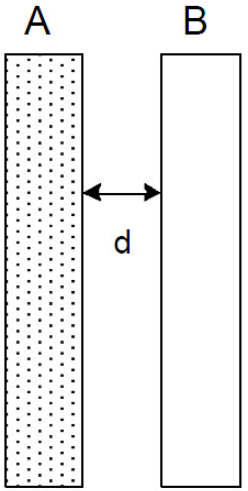


Fig 4

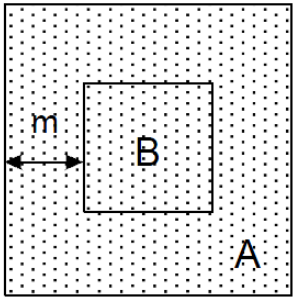


Fig 5

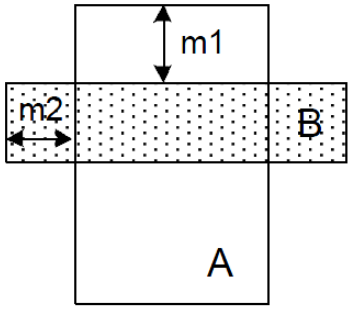


Fig 6

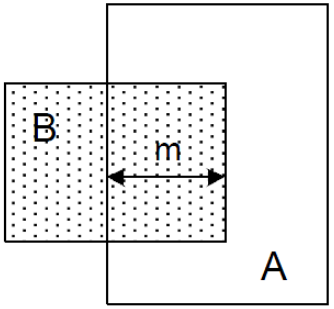
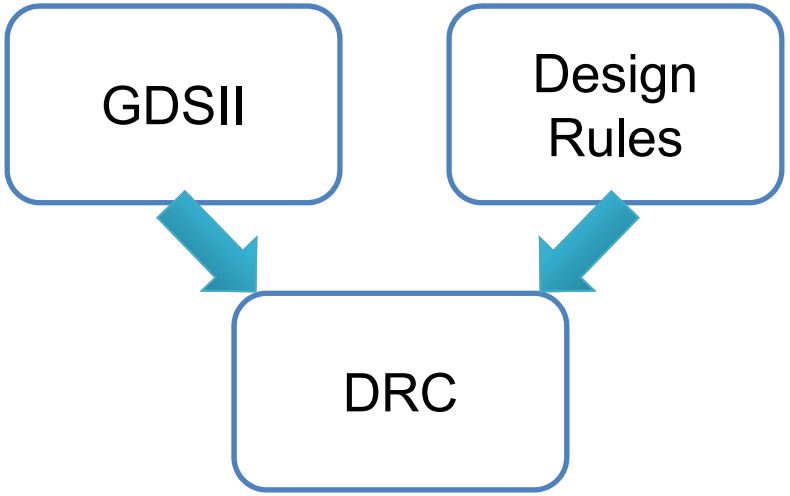


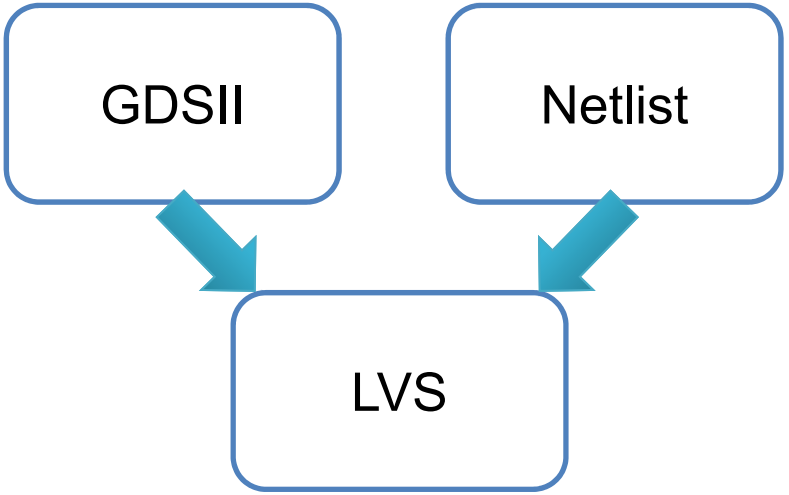
Fig 7

Physical Verification

DRC: Design Rule Check

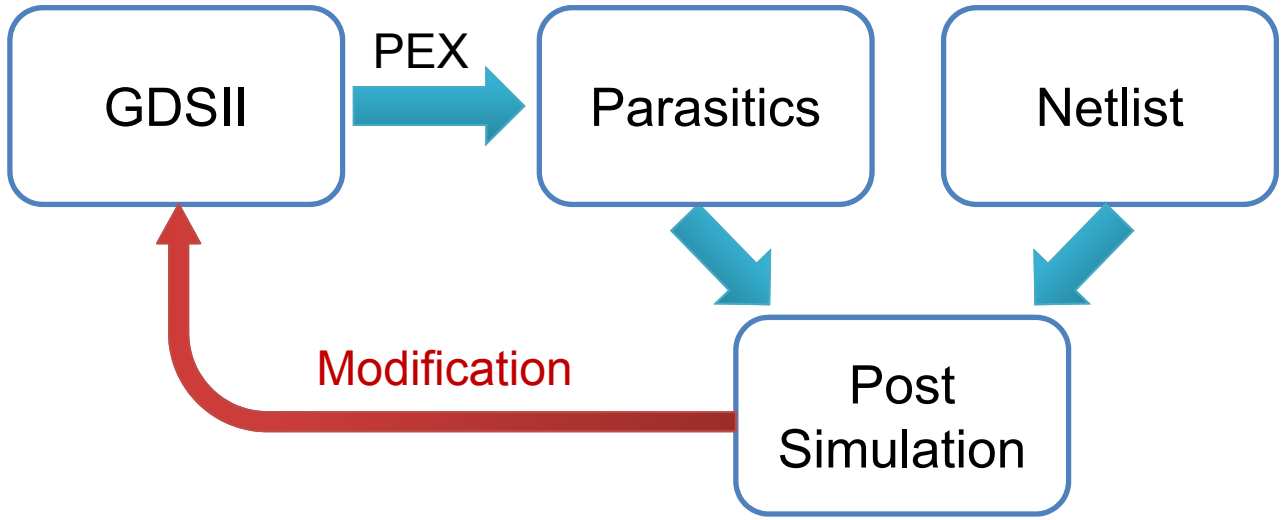


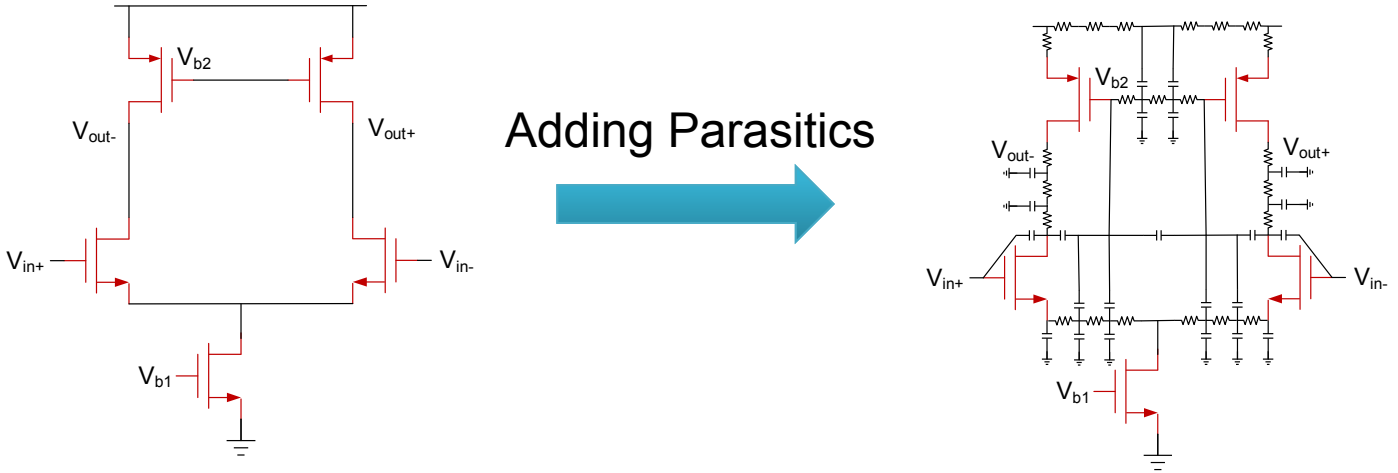
LVS: Layout Versus Schematic



Post Simulation

PEX: Parasitic Extraction





Layout Design Tools

- Cadence:

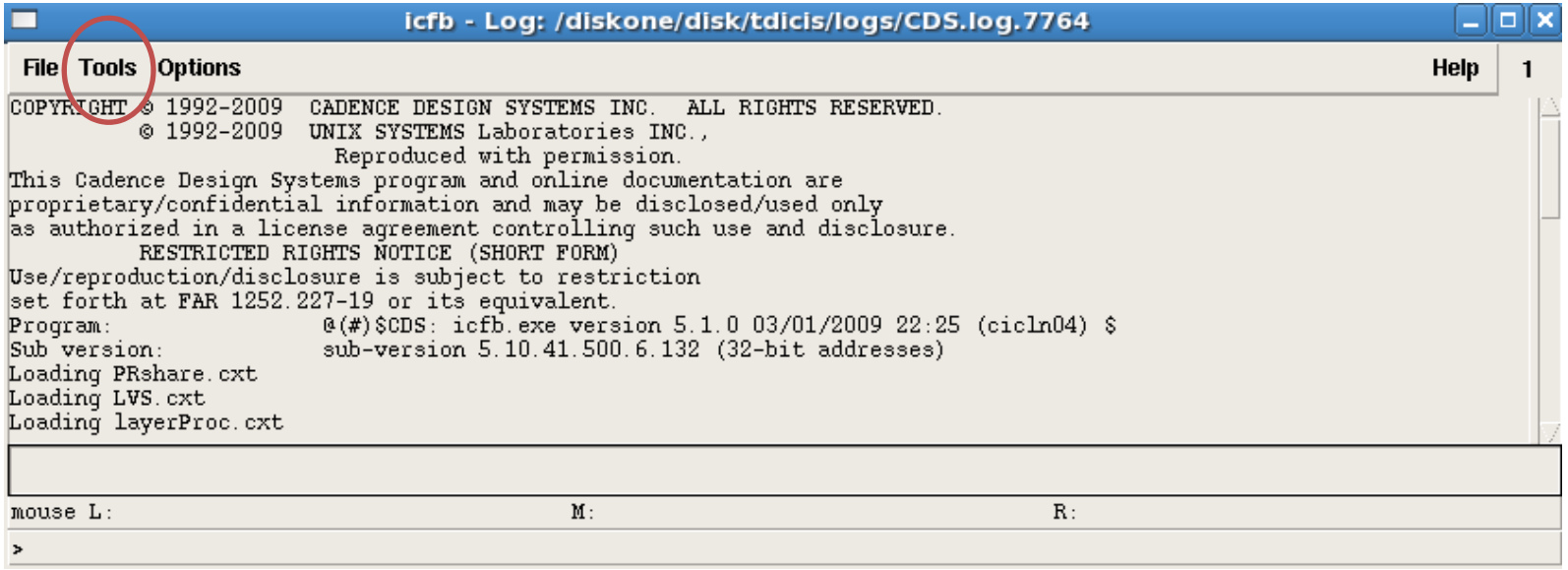
IC development software tools package based on UNIX/Linux platform. The mainstream layout design tool used in the industry is the Virtuoso Layout Editor in Cadence software packages.

- Mentor:

The mainstream layout physical verification tool used in the industry is the Calibre in Mentor software packages.

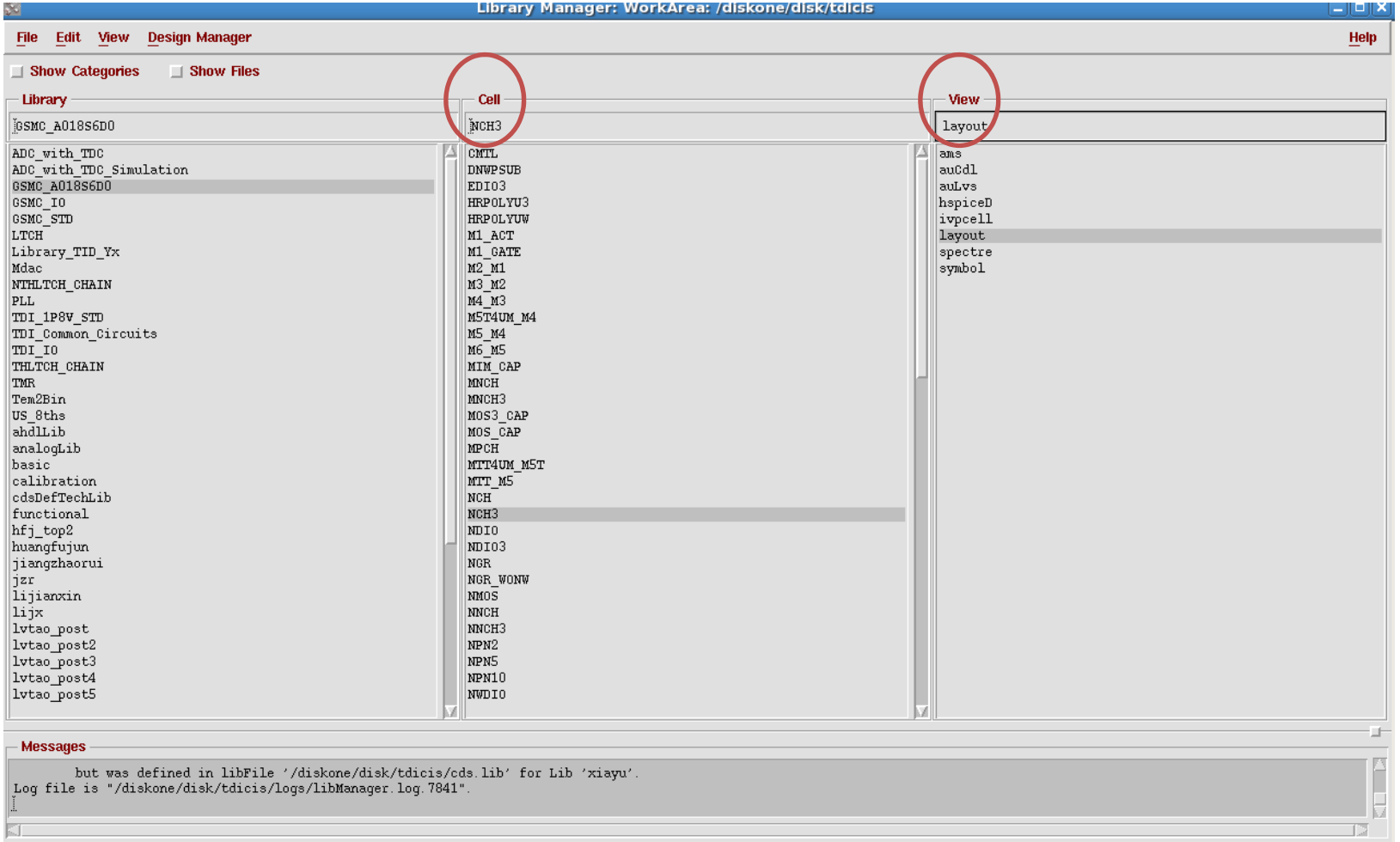
Instructions of Cadence Virtuoso

Type “icfb &” in the terminal of linux OS to start Command Interpreter Window (CIW).



Instructions of Virtuoso

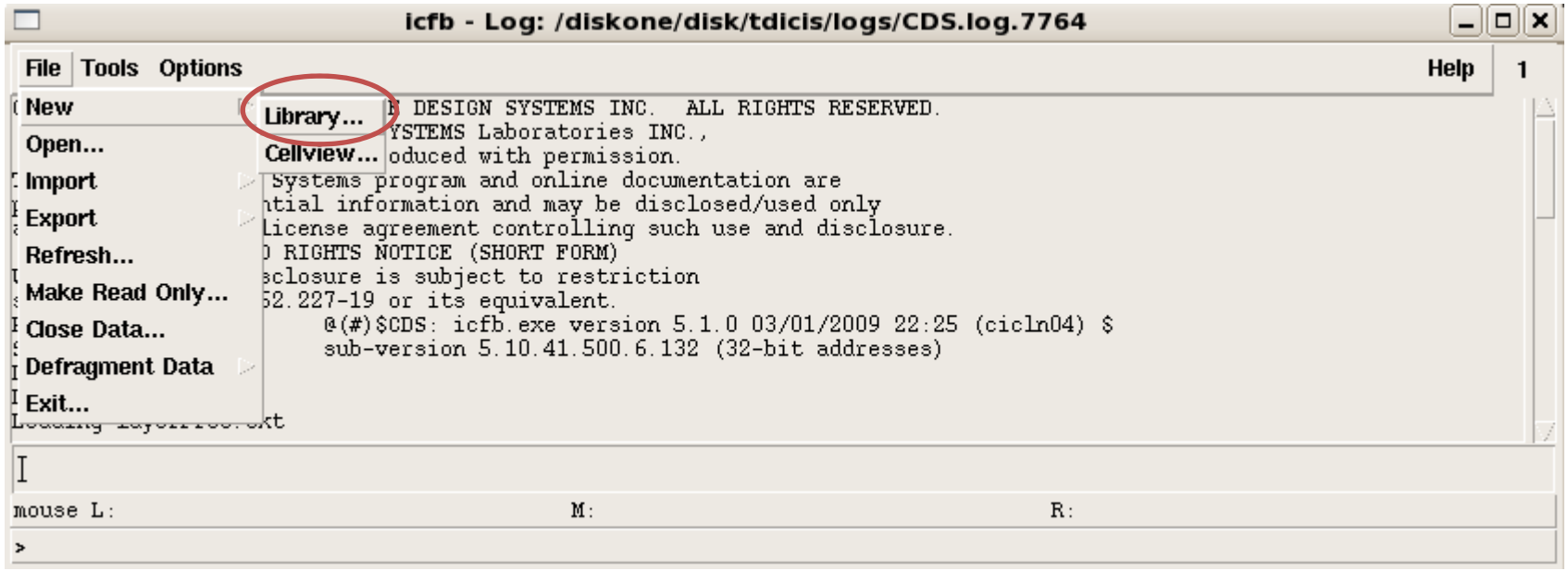
Tools > Library Manager



Instructions of Virtuoso

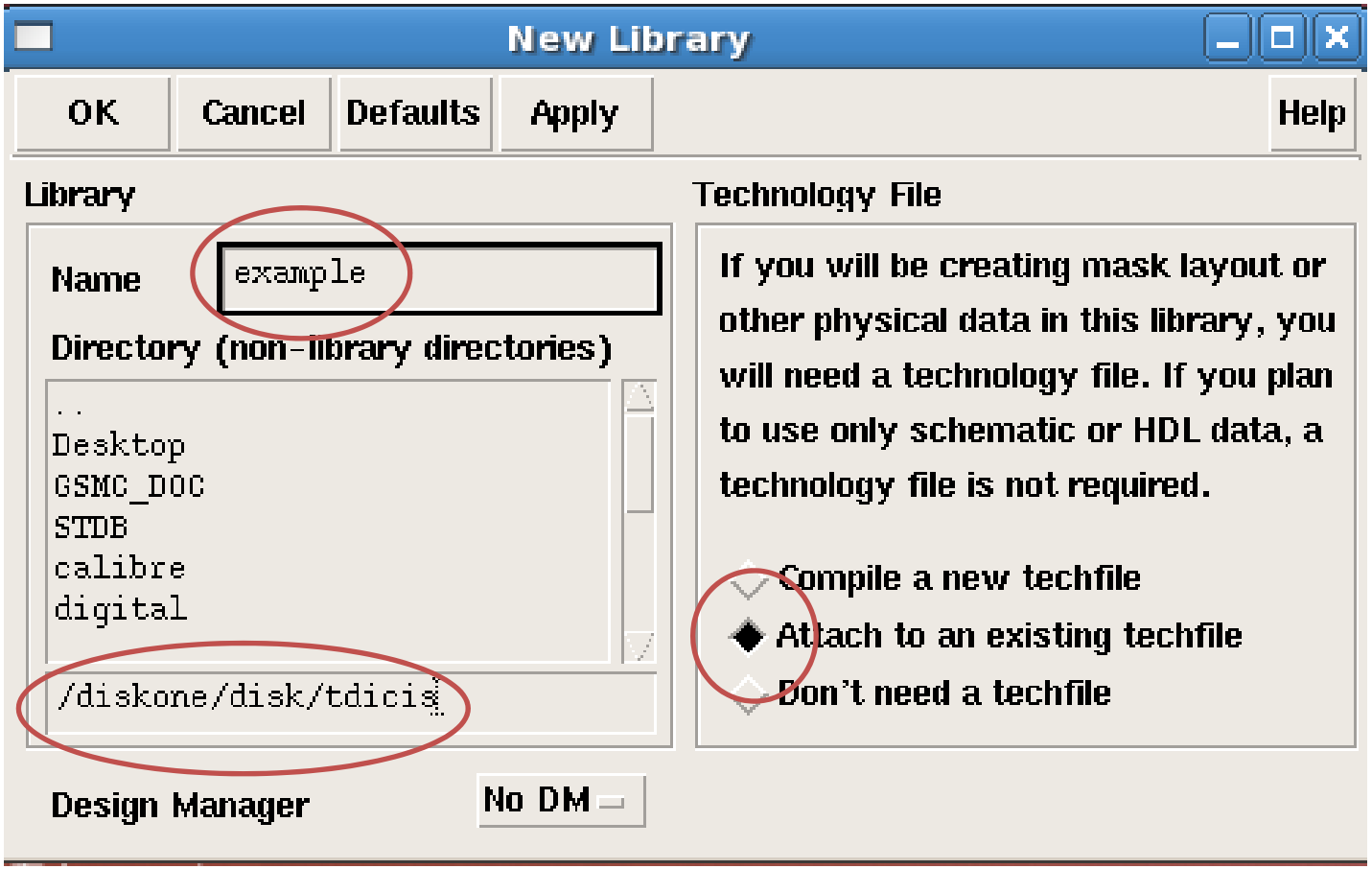
Create a new library with the Process Design Kits (PDK).

- PDK is a complete set of building blocks that are needed for any full custom integrated circuit design and layout. PDK Supports the whole full custom IC design flow from schematic and layout creations to post-layout simulations.



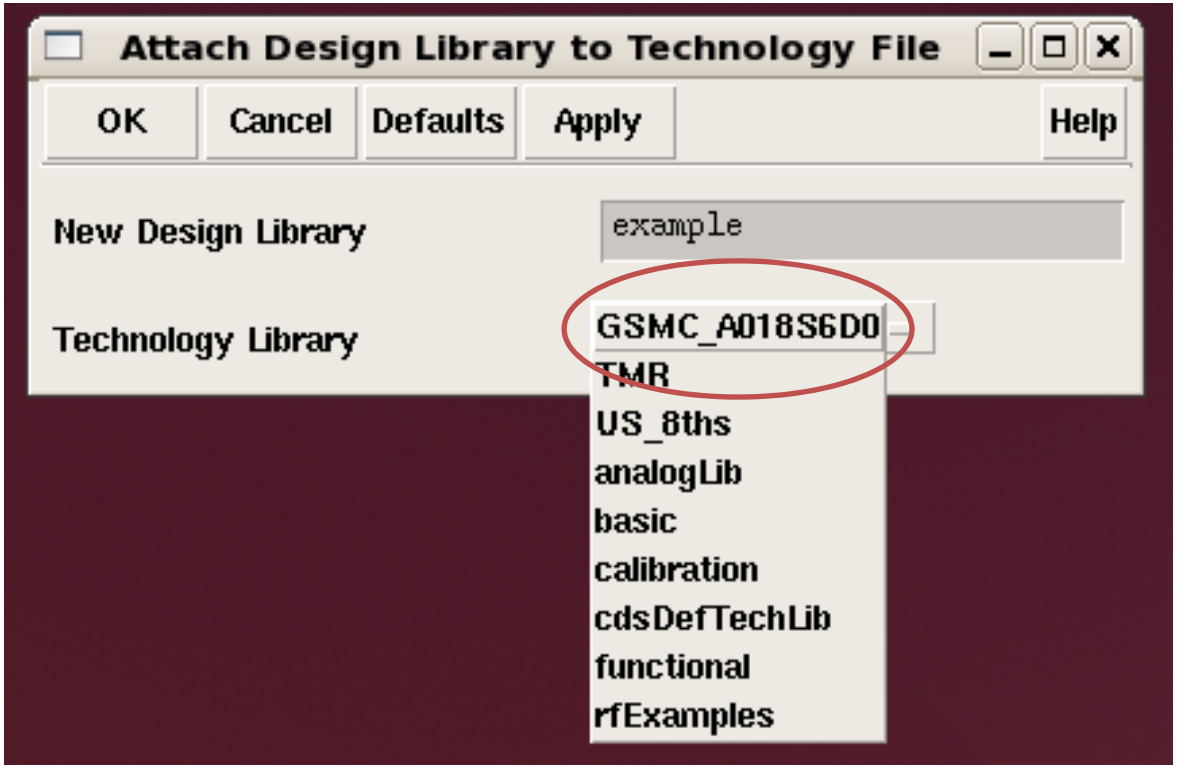
Instructions of Virtuoso

1. Type the name of the new library that you want to create.
2. Choose the directory of the library.
3. Attach the library to a techfile.



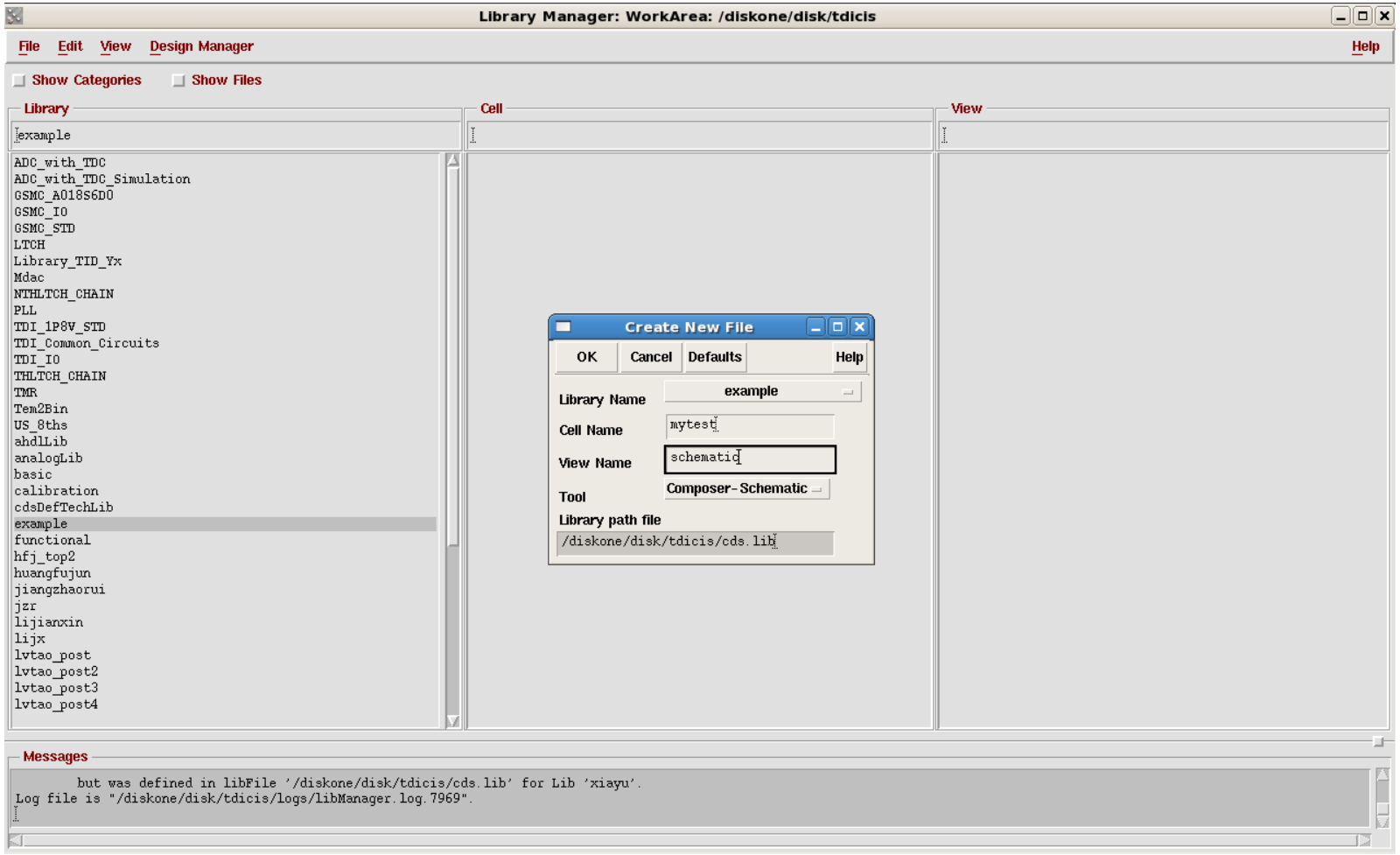
Instructions of Virtuoso

Choose the techfile: GSMC_A018S6D0



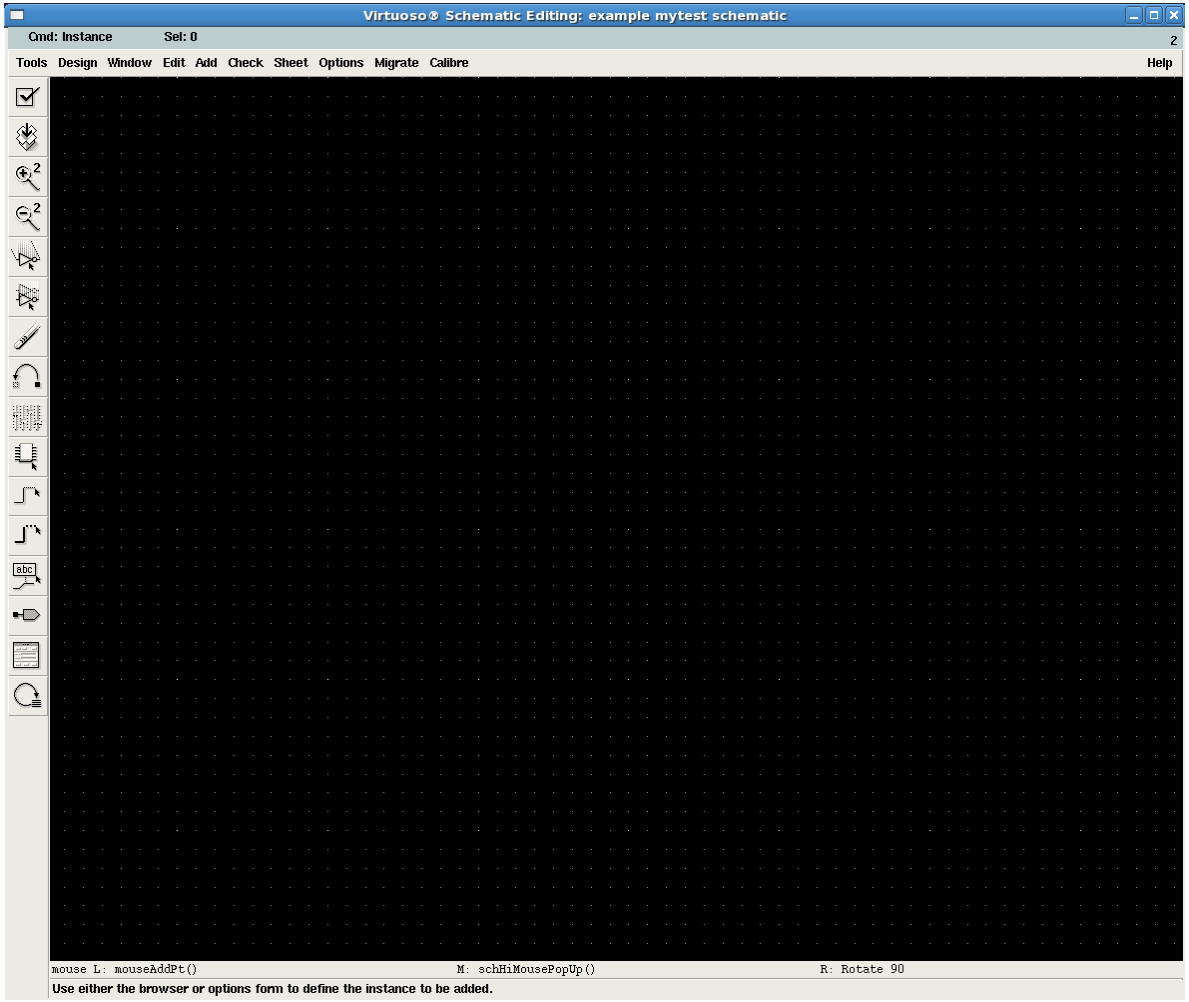
Instructions of Virtuoso

Create Schematic: File > New > Cell View



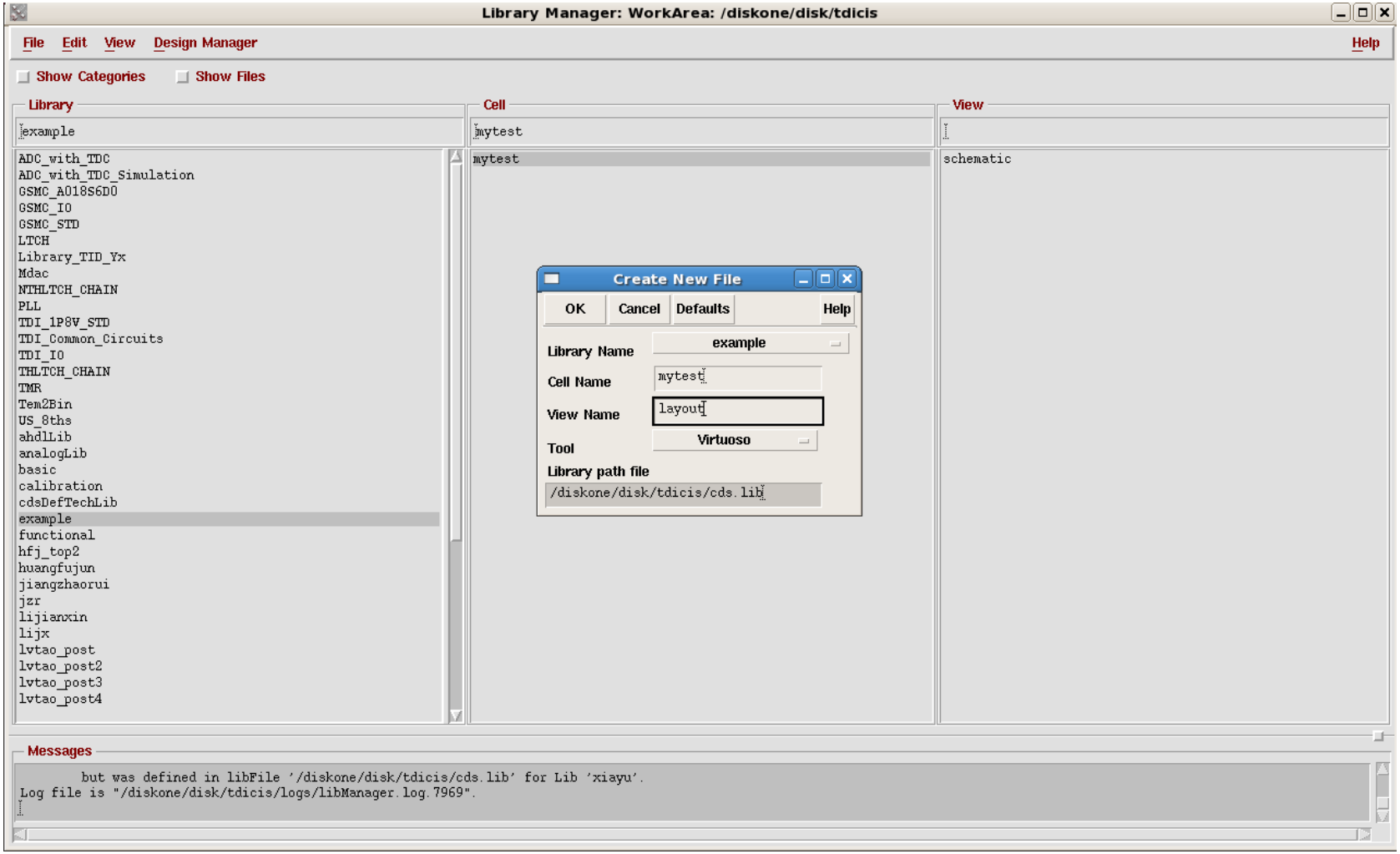
Instructions of Virtuoso

Schematic Editor



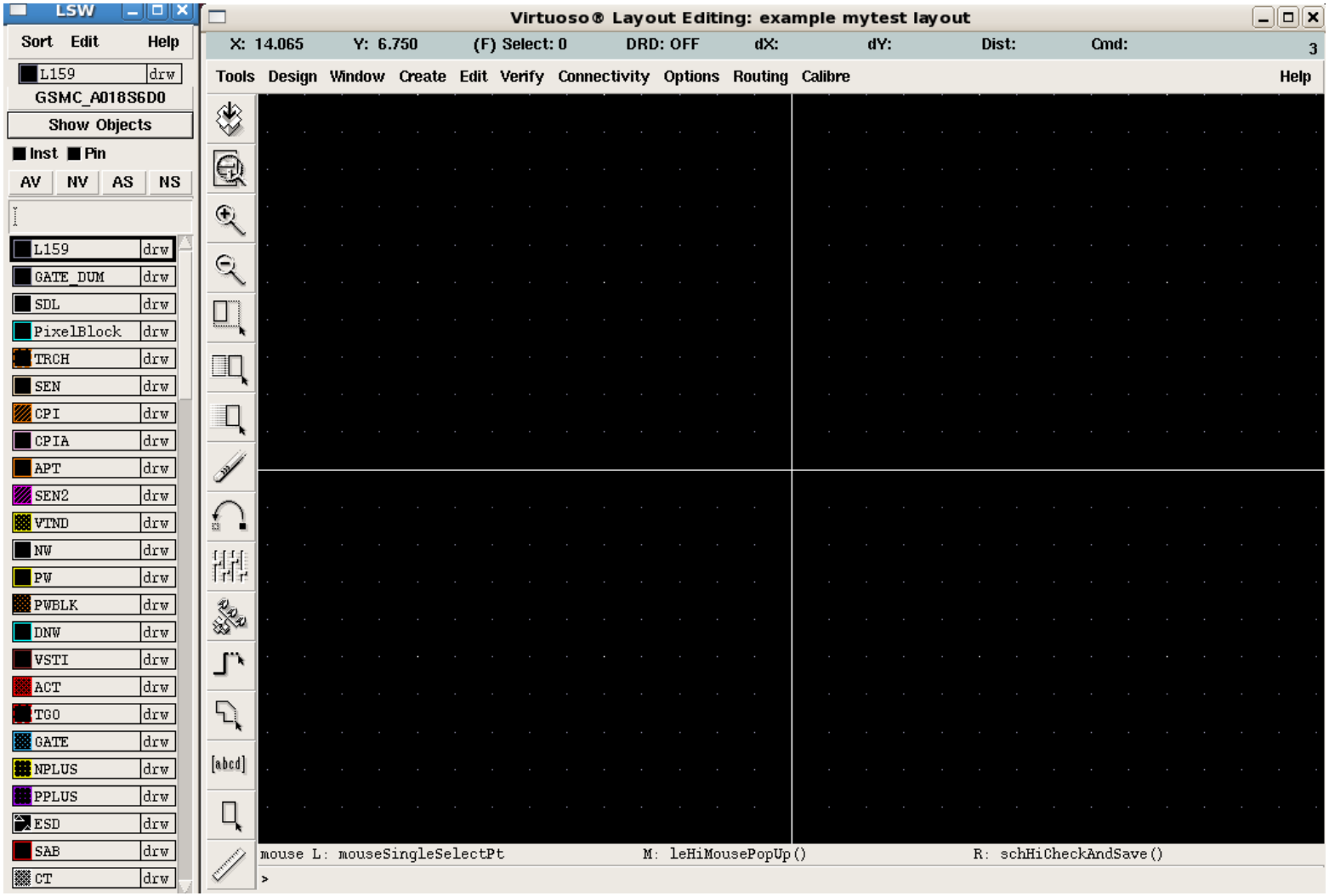
Instructions of Virtuoso

Create Layout: File > New > Cell View

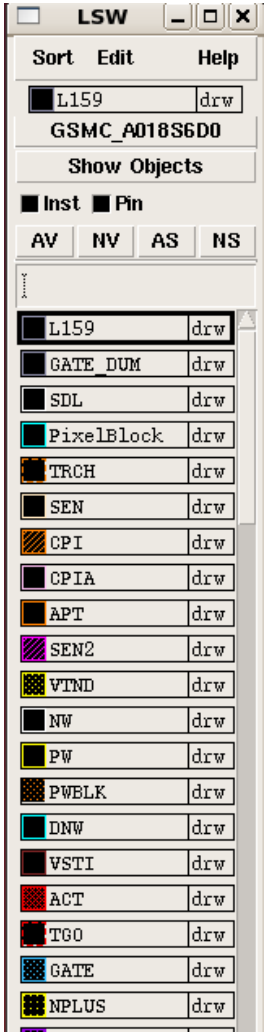


Instructions of Virtuoso

Virtuoso Layout Editor



Instructions of Virtuoso



Layer Selection Window (LSW)

Set drawing layer

Set layer visible

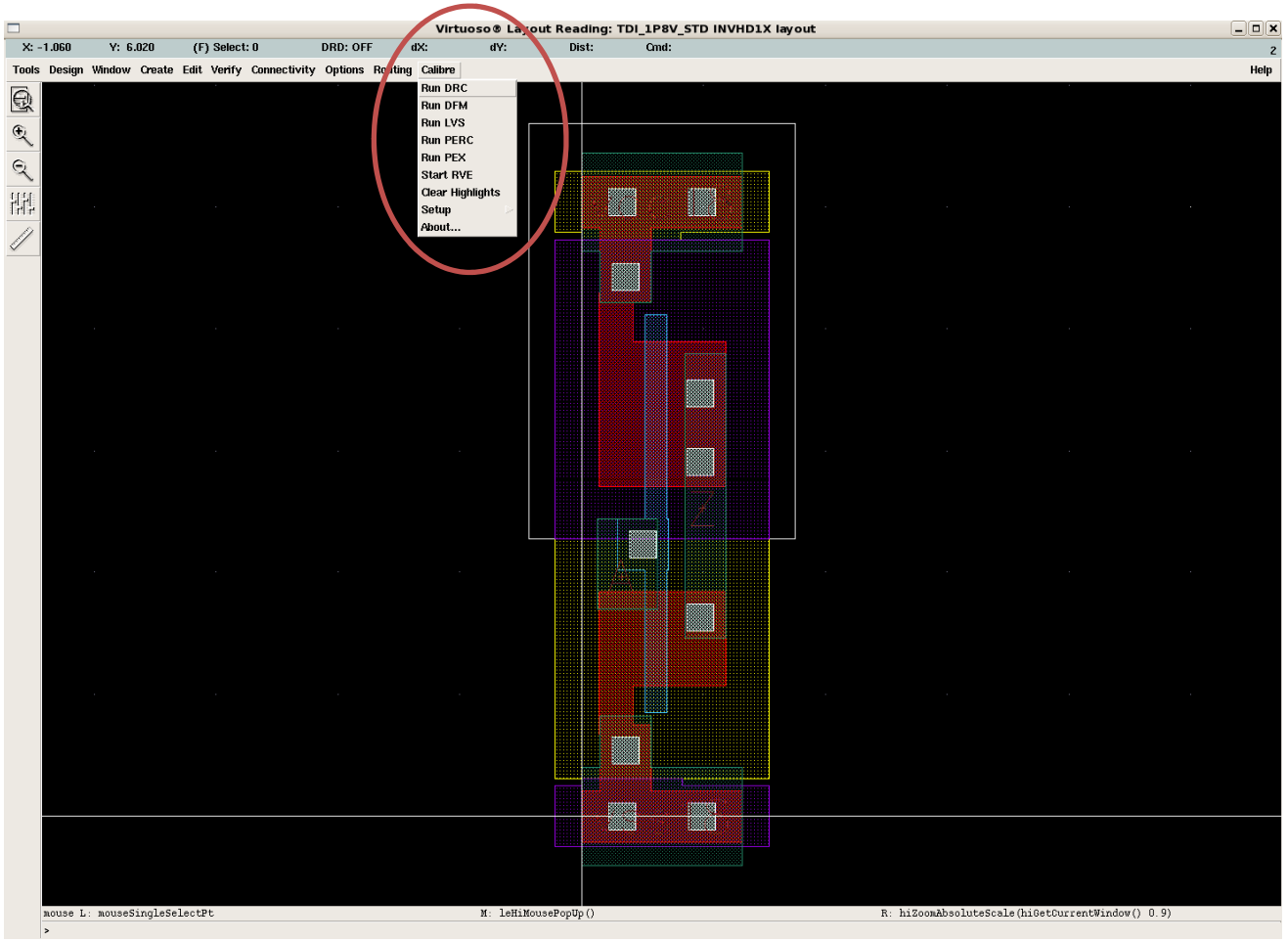
Set layer selectable

Set valid layer

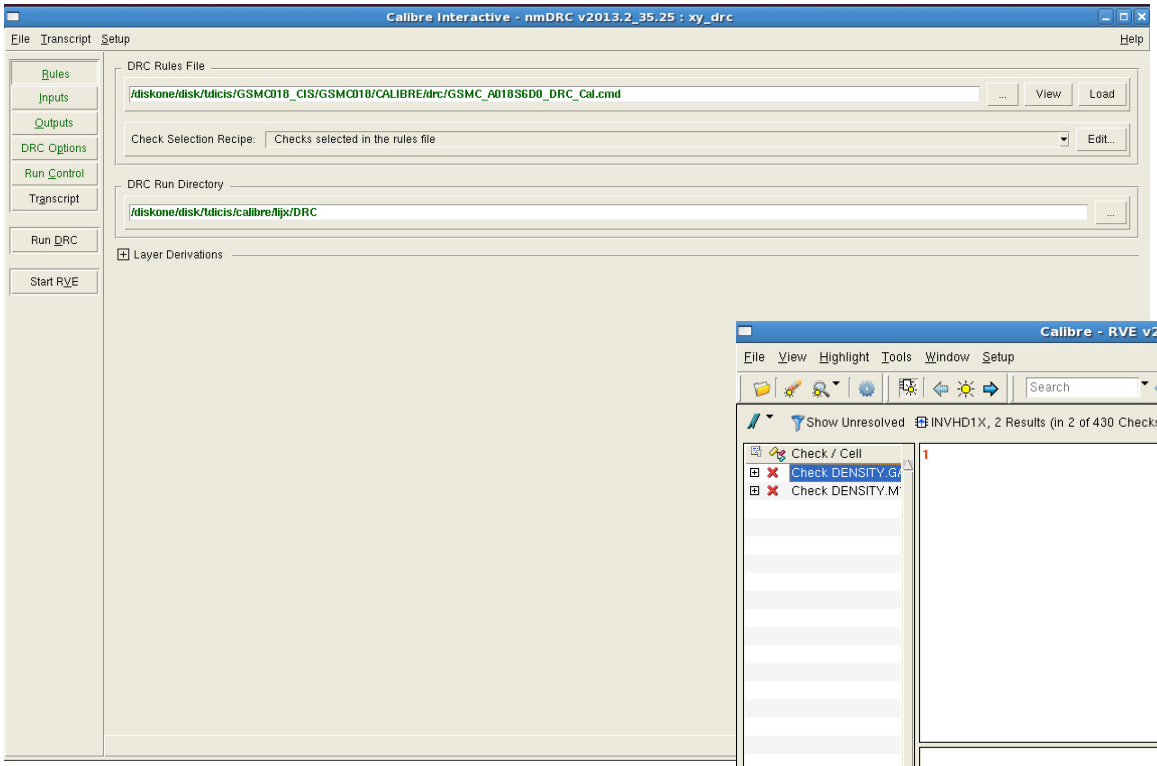
…

Instructions of Calibre

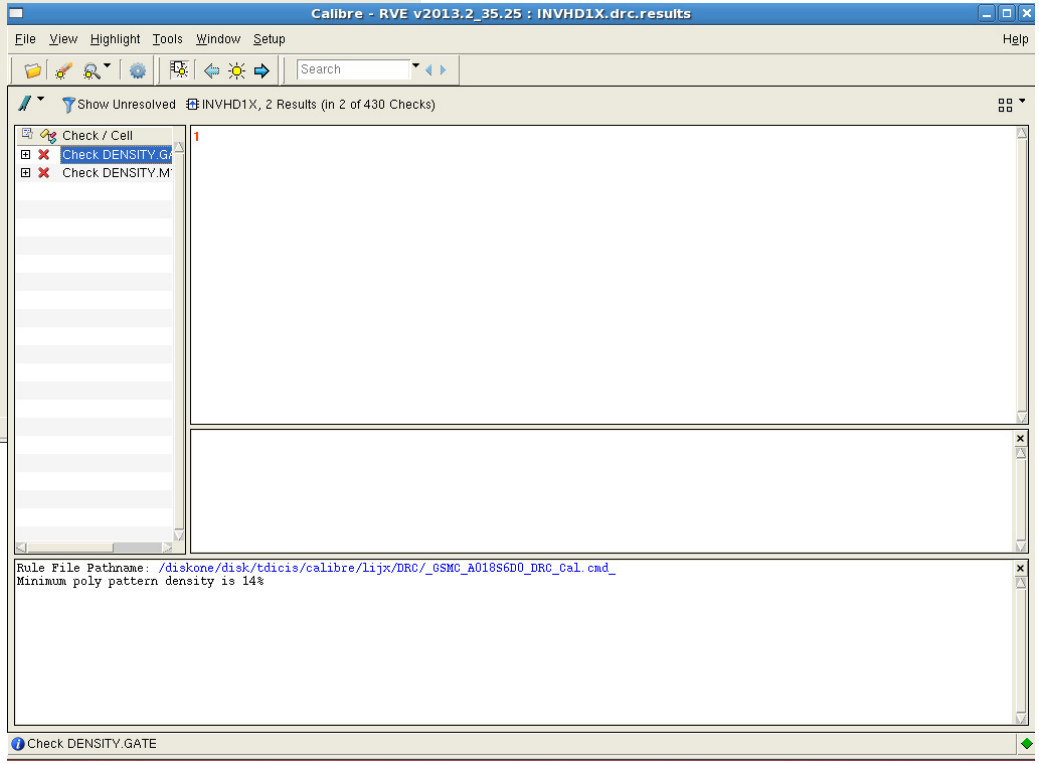
Start Calibre DRC, LVS… from here.



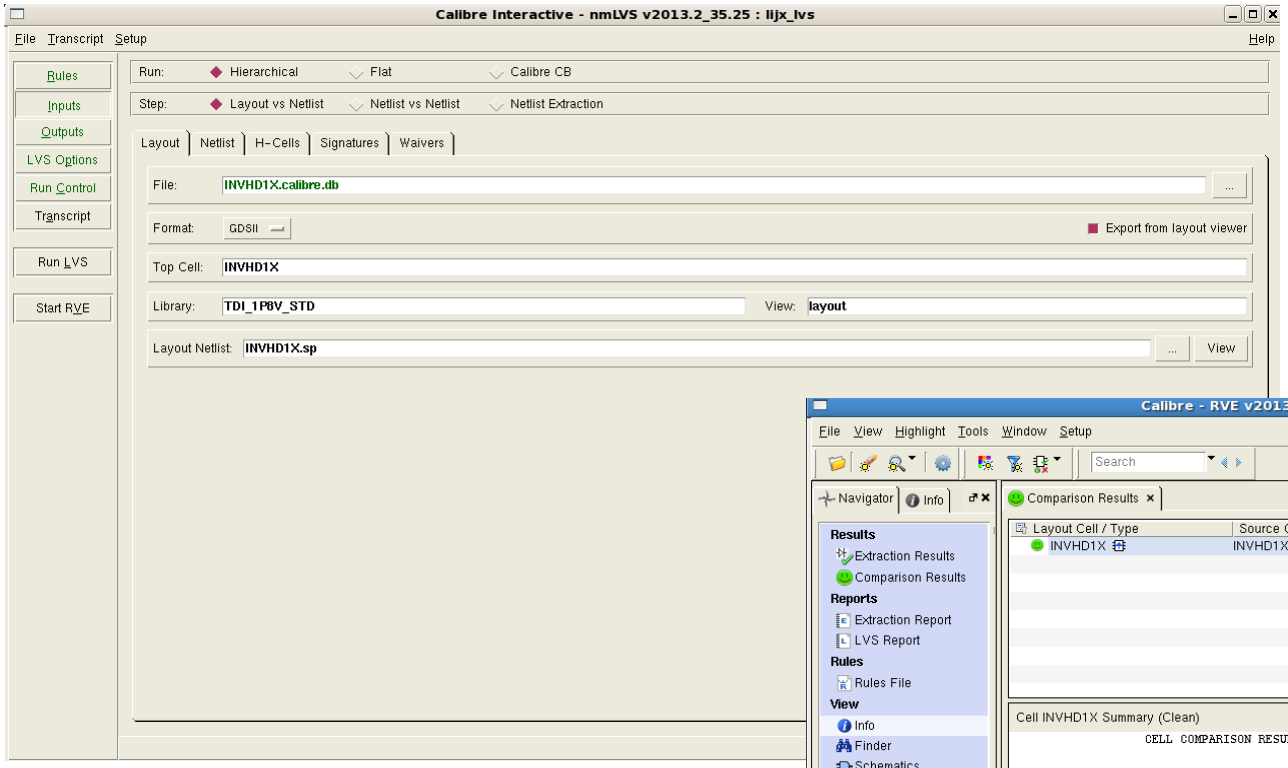
Instructions of Calibre



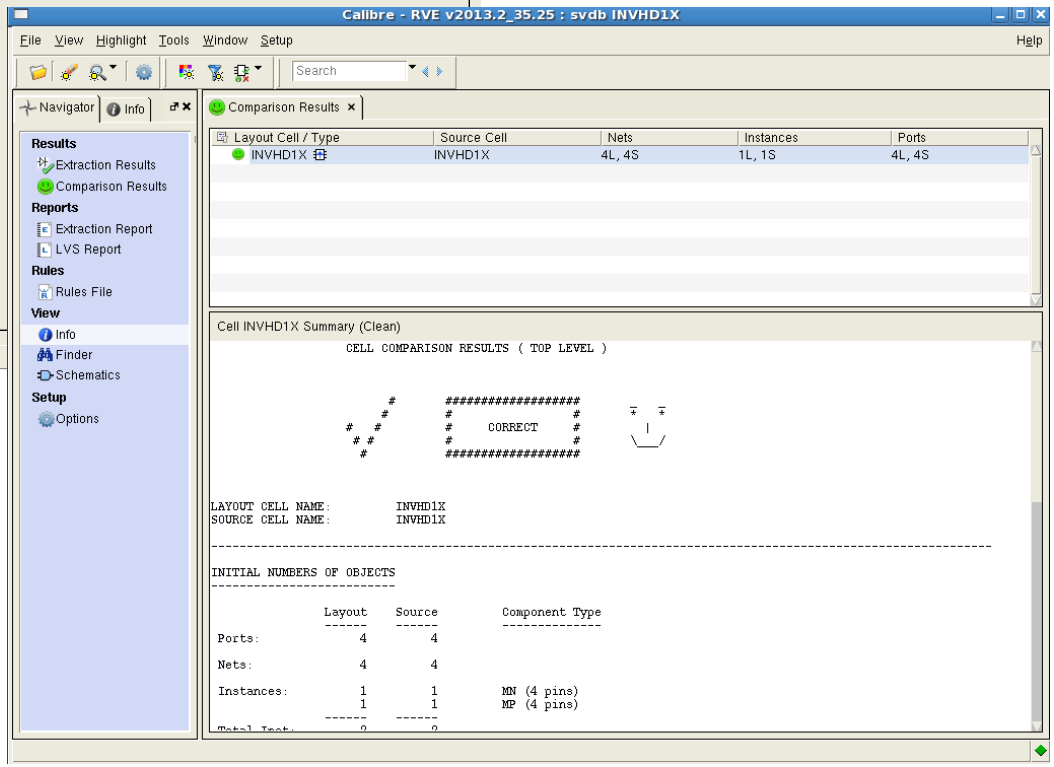
DRC



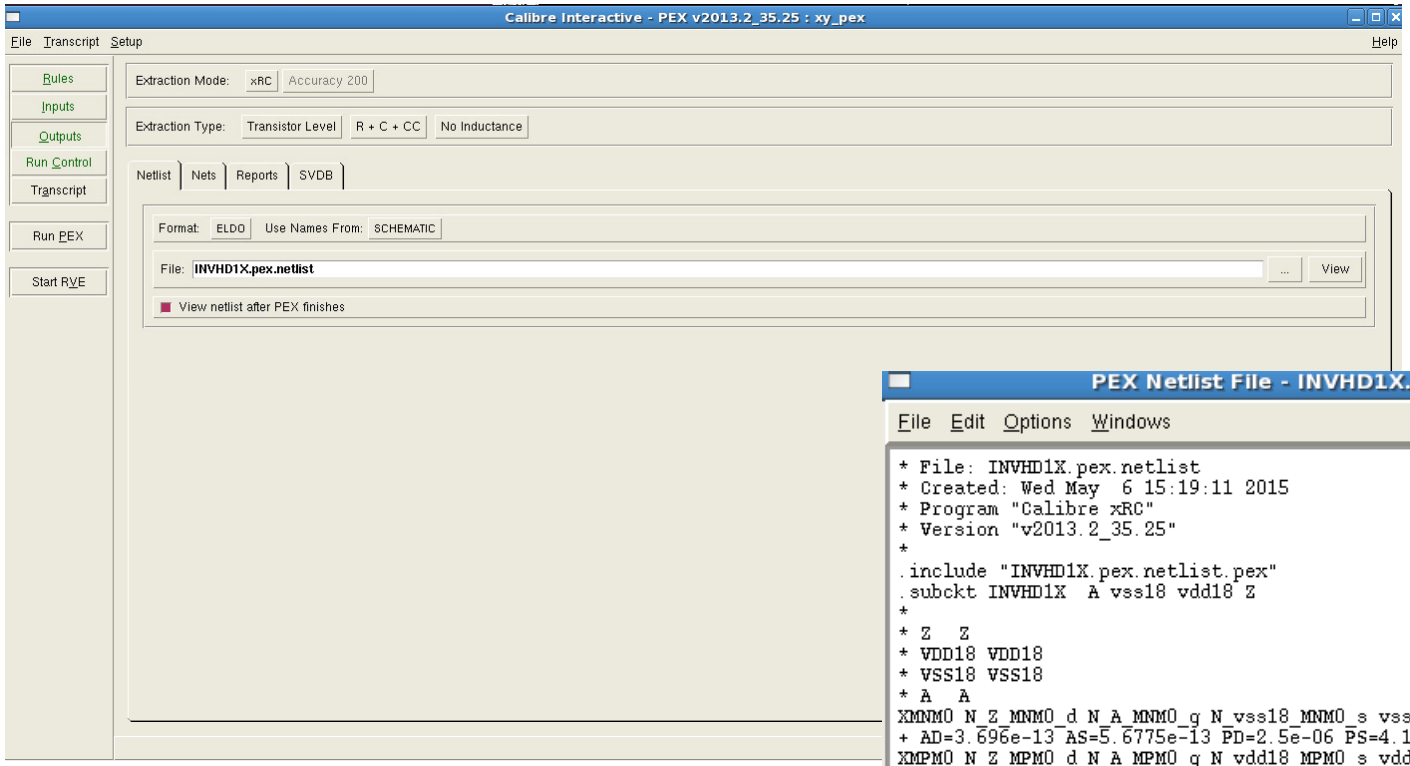
Instructions of Calibre



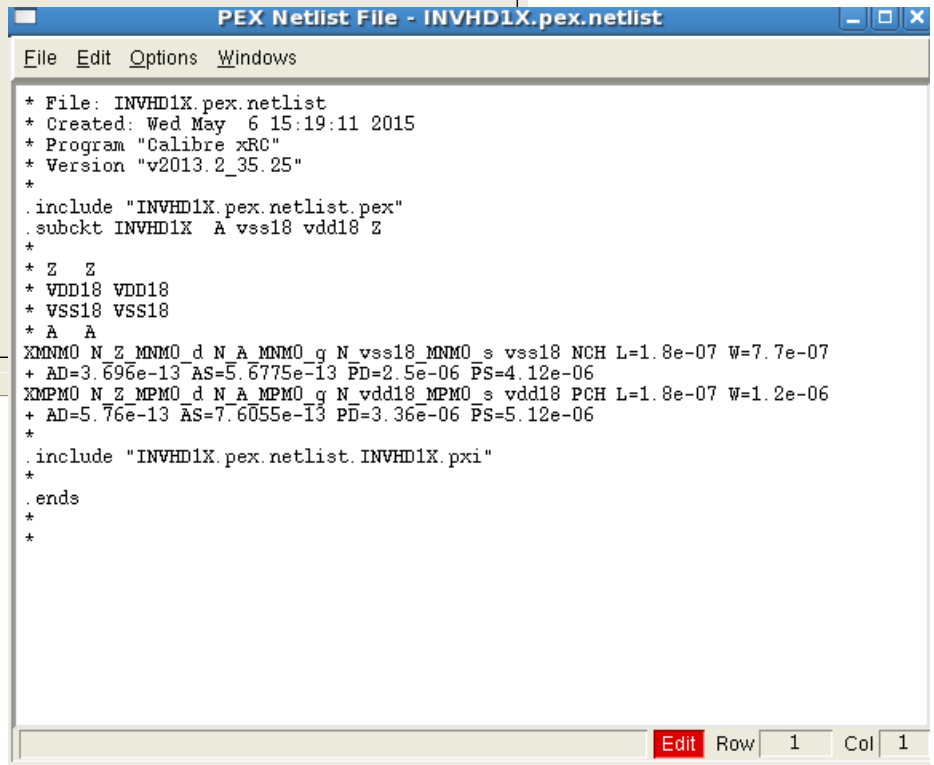
LVS



Instructions of Calibre



PEX



Computer Lab

1. Get familiar with the Virtuoso design environment.
2. Create a library.
3. Create a schematic cellview.
4. Create a layout cellview.
5. Get familiar with the Calibre verification environment, and run DRV, LVS and PEX with the example library “caliber_experiment”.

集成电路版图设计技术

Layout Techniques of the Integrated Circuit

聂凯明

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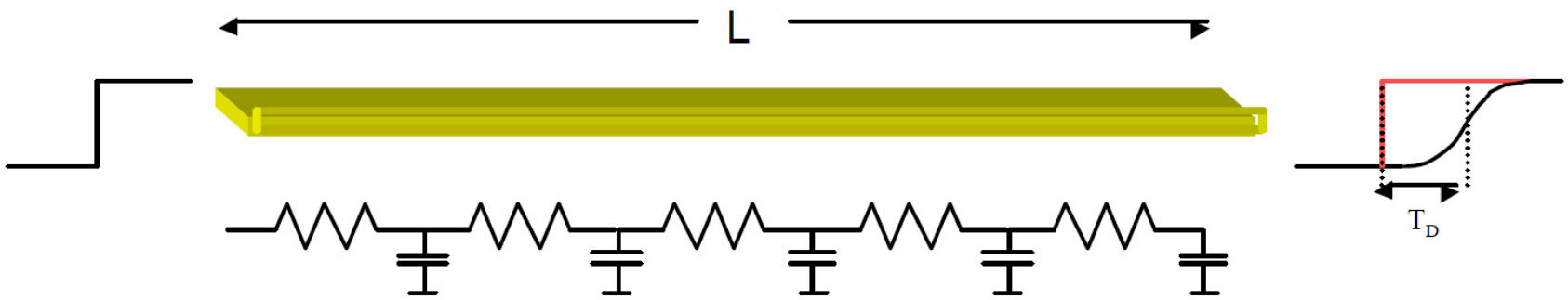
Lecture 2:

Basic Drawing Layers and Failure Mechanisms

The Metal Layers

The Metal layers are used to connect circuit elements (transistors, capacitors, resistors…), and the metal is either aluminium or copper in a CMOS process.

There are parasitic capacitance and resistance in metal layers. The distributed resistance and capacitance introduce a dispersion of the signal.



$$T_D = \frac{1}{2} R_U C_U L^2$$

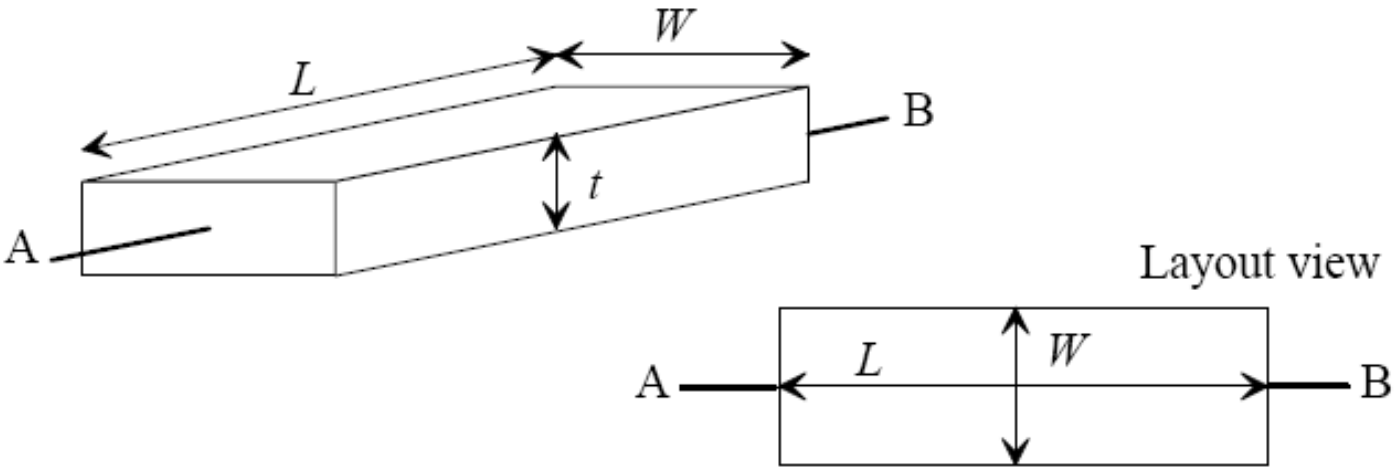
R_U, C_U resistance and capacitance per unit length

The Metal Layers

The parasitic resistance between A and B is: $R = \frac{\rho}{t}\frac{L}{W}$

It can be transformed to: $R = R_{square}\frac{L}{W} \rightarrow R_{square} = \frac{\rho}{t}$

R_{square} is the metal sheet resistance, which is used to calculate a parasitic resistance.



The Metal Layers

If the metal1 sheet resistance is 0.1Ω/square, estimate the resistance of a piece of metal1 1mm long and 200nm wide.

1: The line consists of 1000/0.2=5000 squares of metal1.

2: To calculate the resistance of the metal line:

$$R = \frac{0.1\Omega}{square} 5000 = 500\Omega$$

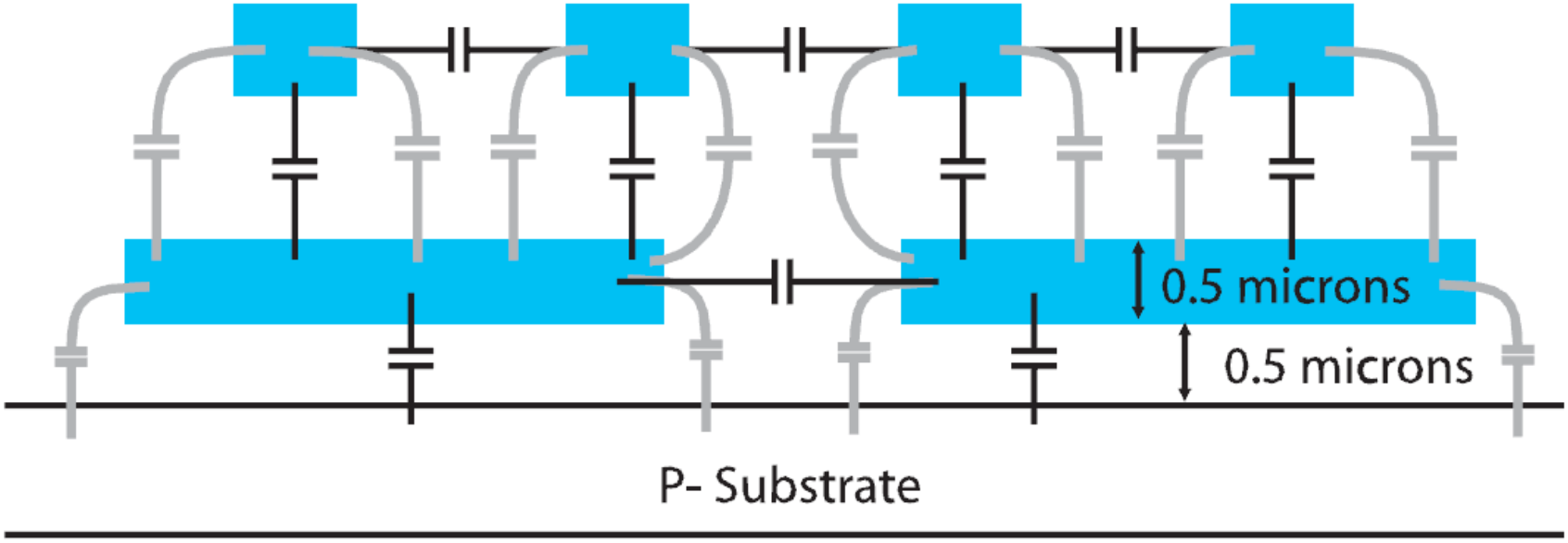
The Metal Layers

Typical parasitic capacitances in a CMOS process.
$1aF=10^{-18}F$

	Plate Cap. aF/μm²			Fringe Cap. aF/μm		
	min	typ	max	min	typ	max
Poly1 to subs. (FOX)	53	58	63	85	88	92
Metal1 to poly1	35	38	43	84	88	93
Metal1 to substrate	21	23	26	75	79	82
Metal1 to diffusion	35	38	43	84	88	93
Metal2 to poly1	16	18	20	83	87	91
Metal2 to substrate	13	14	15	78	81	85
Metal2 to diffusion	16	18	20	83	87	91
Metal2 to metal1	31	35	38	95	100	104

The Metal Layers

Capacitance is everywhere. Everything is talking to everything else, through some kind of a capacitance.



The Metal Layers

If the unit plate and fringe parasitic capacitance of a metal1 with thickness of 1um are 23aF/um2 and 79af/um respectively, estimate the capacitance of a piece of metal1 1mm long and 200nm wide and the delay through this metal line

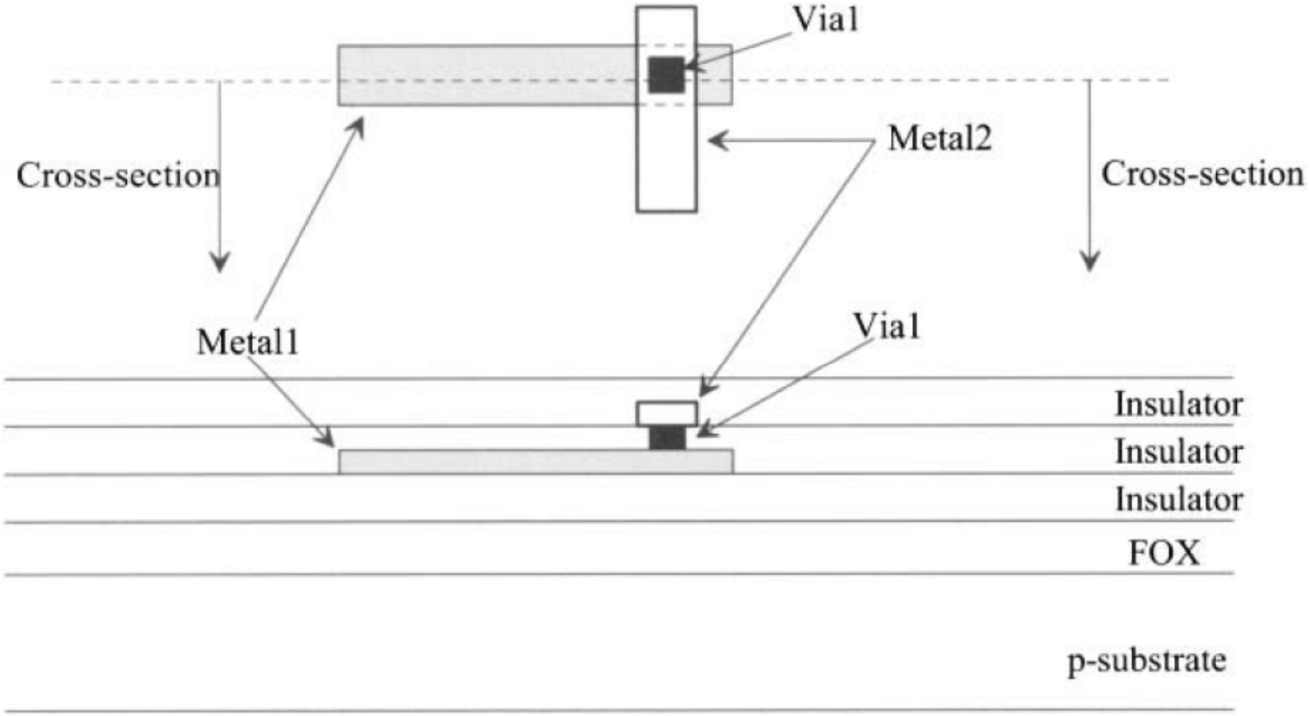
1: C_{total}=(1000*0.2)*23aF+(1000*1*2)*79aF=162fF

2: R_{total}=500Ω

3: Td=0.5R_{total}*C_{total}=40.5ps

The Via Layers

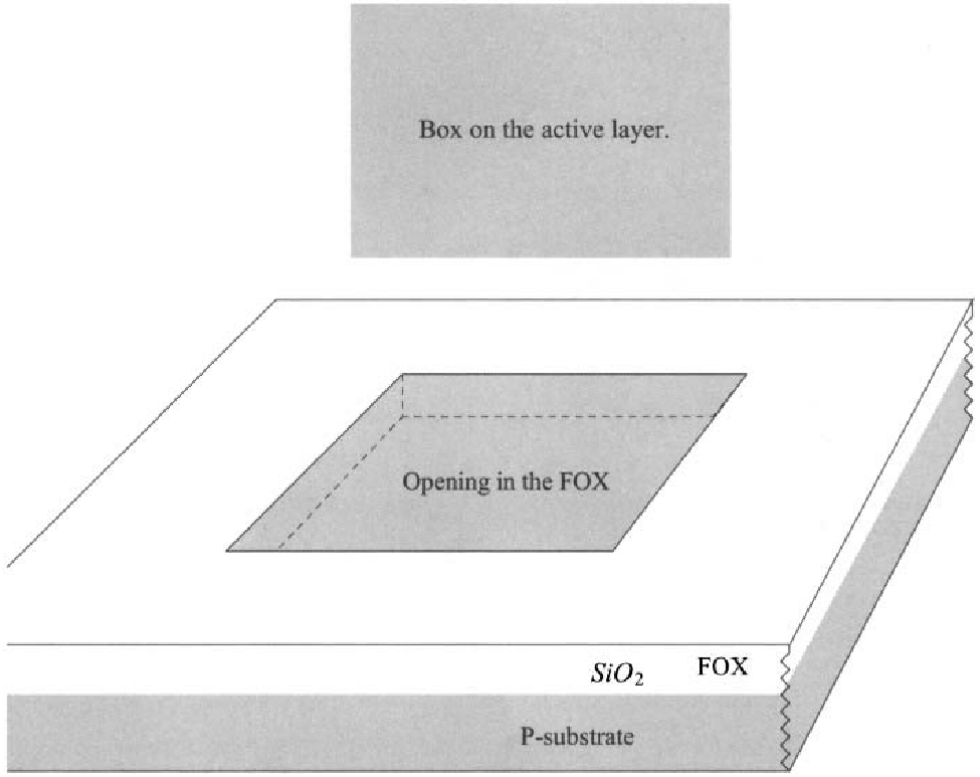
The via layers are used to connect adjacent metal layers.



Note that if we were to use more than two layers of metal, then via2 would connect metal2 to metal3, via3 would connect metal3 to metal4, etc.

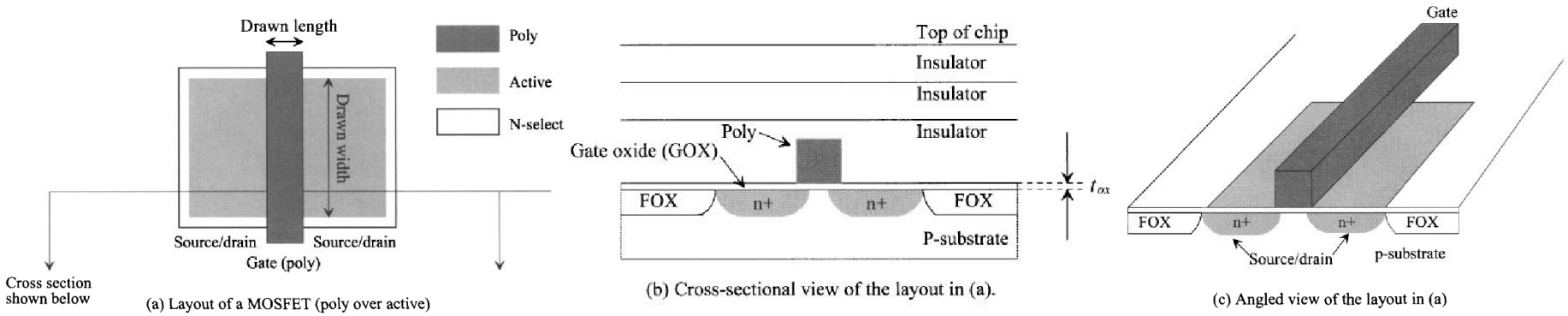
The Active Layers

The box is drawn on the active layer and indicates where to open a hole in the field oxide(FOX). These openings are called active areas. The MOSFETs are fabricated in the bulk in these active openings.



The Poly Layers

The poly layer is used for MOSFET formation. Draw poly over active produce a MOSFET layout. Note that the gate of the MOSFET is formed with the polysilicon.



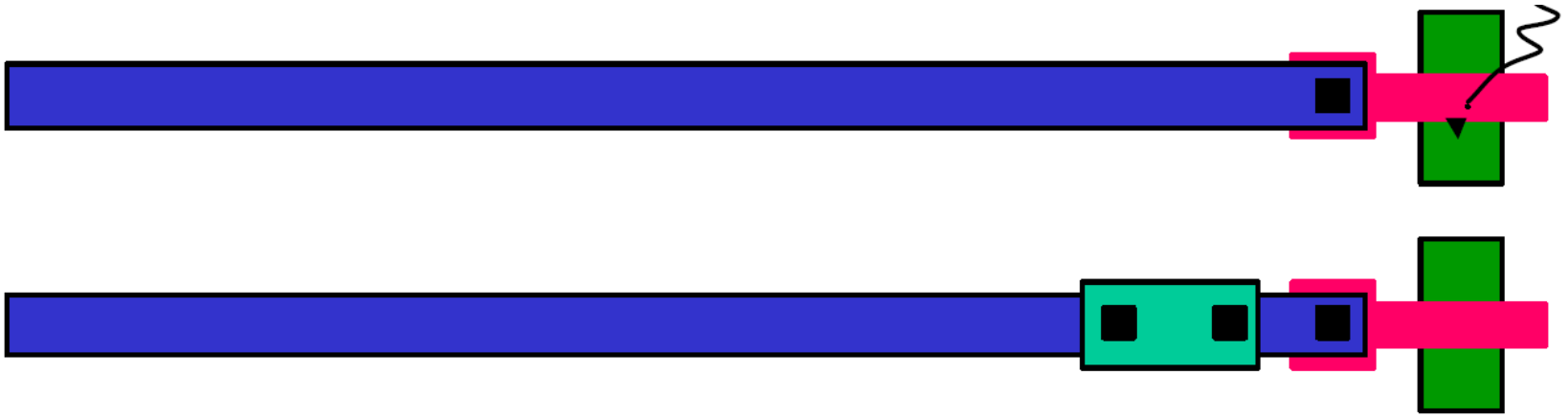
The poly layer can also be used, like metal1, as a wire. The main limitation when using the poly layer for interconnection is its sheet resistance, which can be on the order of 200Ω/square, so it is only suitable for short interconnection.

Basic Drawing Layers in GSMC_A018S6D0

Abbreviation	Description
Baseline Layers	
ACT	Active region
NW	N-well implant region
NWDMY	Dummy layer to define the NW resistor region
TGO	Thick GATE Oxide region for 3.3V device
GATE	Poly GATE region
PPLUS	P+ S/D implant region
RNDMY	Dummy layer to define the N-type poly resistor with medium sheet resistance
NPLUS	N+ S/D implant region
RPDMY	Dummy layer to define the P-type poly resistor with medium sheet resistance
SAB	Salicide Block region for ESD device and poly resistor & diffusion resistor
CT	Contact
M1	Metal 1
MV1	Metal Via 1
M2	Metal 2
MV2	Metal Via 2
M3	Metal 3
MV3	Metal Via 3
M4	Metal 4
MV4	Metal Via 4
M5	Metal 5
MV5	Metal Via 5
MT	Metal Top or Metal 6
PA	Passivation opening region

Failure Mechanisms: antenna effect

- Electrical stress can break the gate oxide. Assuming 4×10^6 V/cm dielectric strength, the maximum voltage across a 40 nm oxide is 16 V.
- During dry etching an ionized plasma charges conductors proportionally to their area. For large areas the resulting voltage can be disruptive (antenna effect)



Use of metal2 jumper!

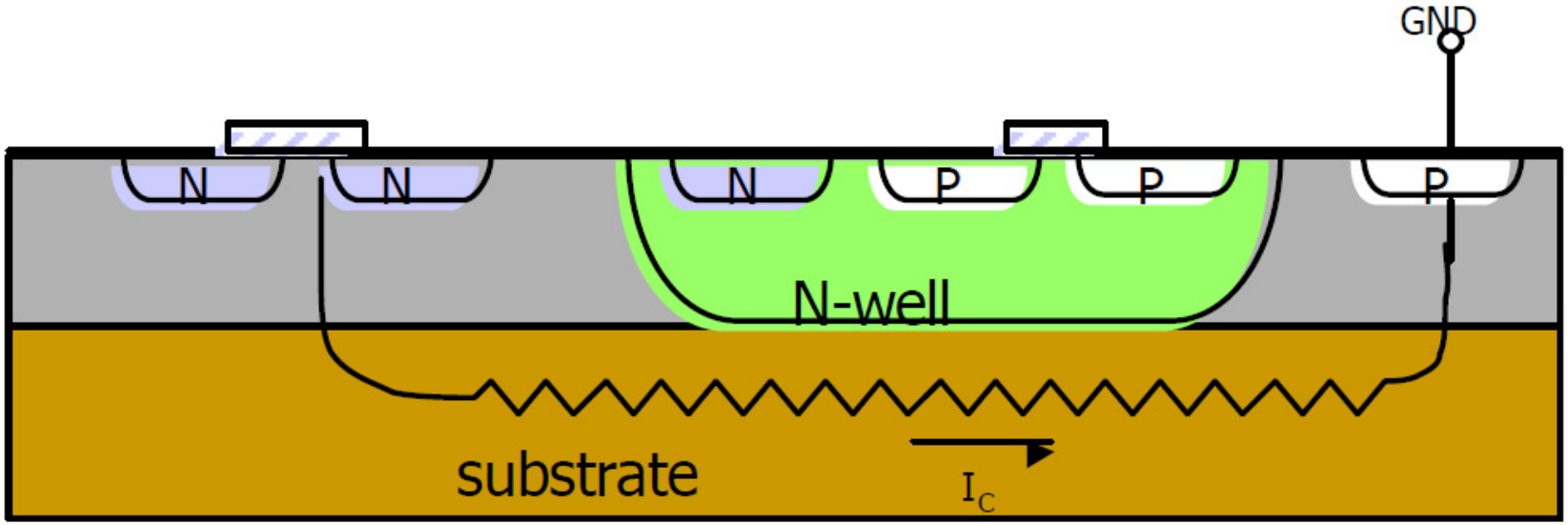
The large metal1 area is etched when the gate is not connected.

Failure Mechanisms: antenna effect

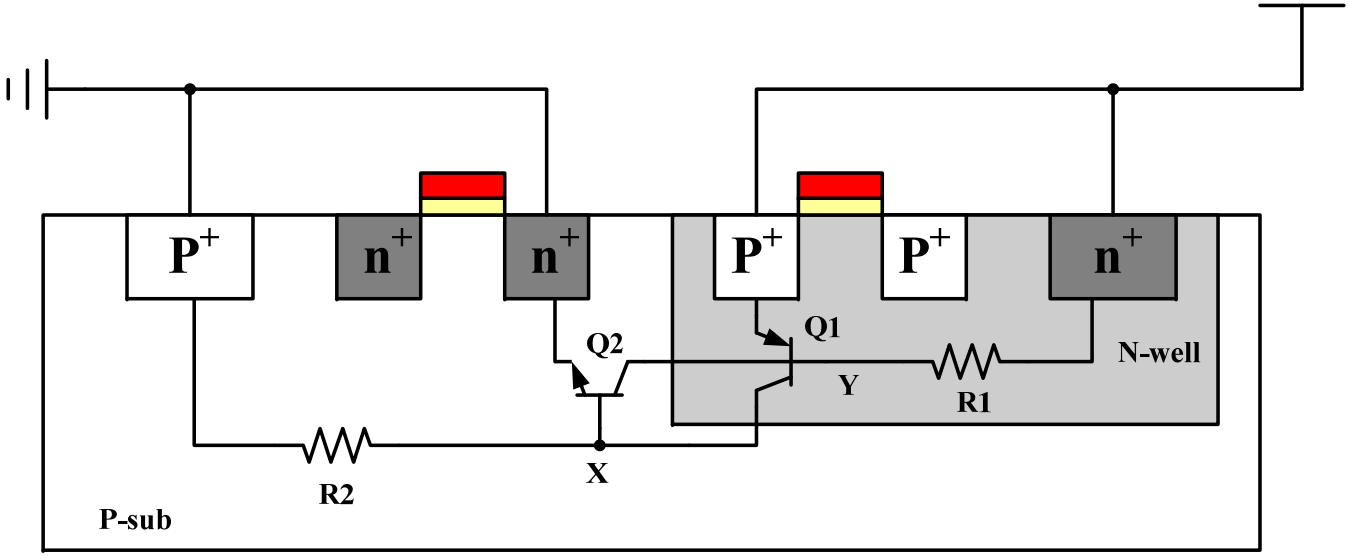
Use PN junction reverse-biased to discharge!

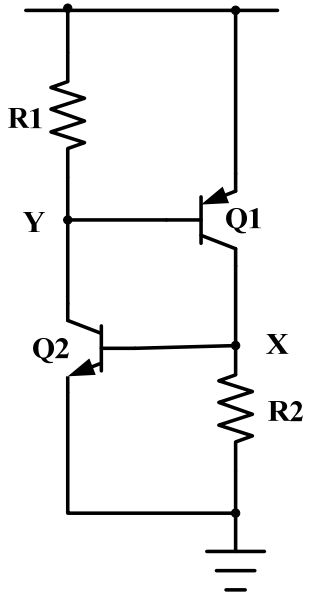
Failure Mechanisms: soft connection

Current in the high resistive substrate lead to significant drop voltages, so we need to bias solidly the substrate.



Failure Mechanisms: Latch-up





Failure Mechanisms: Electro-migration

- Electron flowing through the metal collide with atoms of the lattice. When the current density exceeds a threshold metal atoms begin to move.
- The displacement of atoms can produce a local thinning of the metal or gaps and, eventually, cause an open circuit.
- A fraction of percent of copper added to the aluminum improves the electro-migration resistance.

- Large current requires thick or wide metal lines.

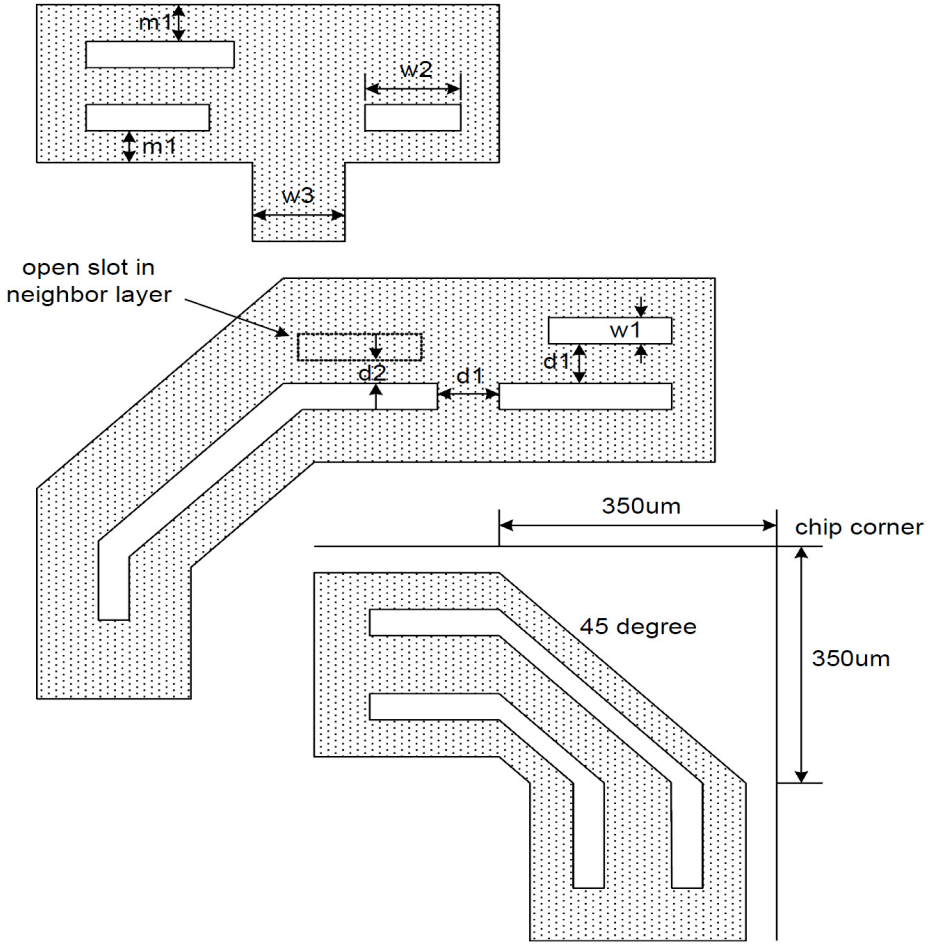
Failure Mechanisms: Electro-migration

Typical current density limit in used layers:

Element	Max Density	Unit
Poly	0.5	mA/um
Metal1	1	mA/um
Metal2	1.5	mA/um
Contact	1	mA/cnt
Via	1.5	mA/via

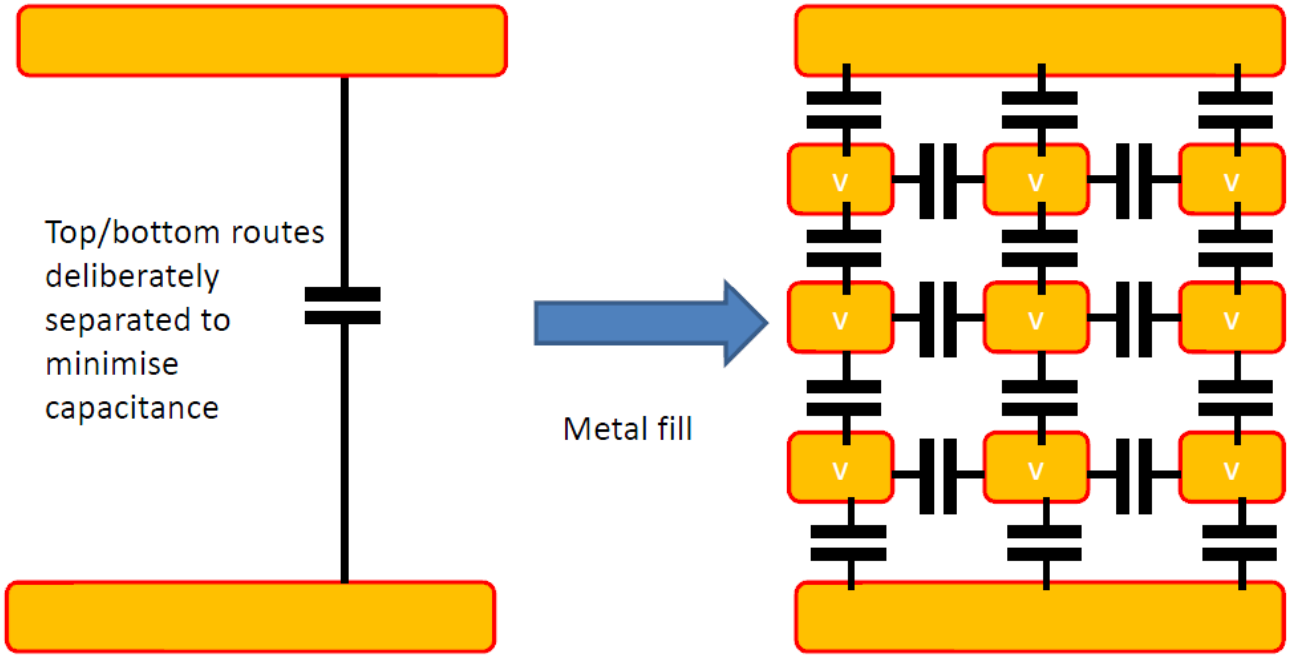
Failure Mechanisms: metal stress

Without metal stress relief design, wide metal layers would crack due to the stress caused by different thermal expansion and contraction coefficients.



Failure Mechanisms: density

To control the process and improve uniformity there are design rules for density of poly, active and metal.
Need to make sure the block doesn't change if Auto fill tools are turned on.



If you want to know the capacitance, put it the metal there yourself, don't let the tools fill it!

Computer Lab

1. Continue the experiment in the last lecture.

2. Get familiar with the GSMC_A018S6D0 technology.

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Layout Techniques of the Integrated Circuit

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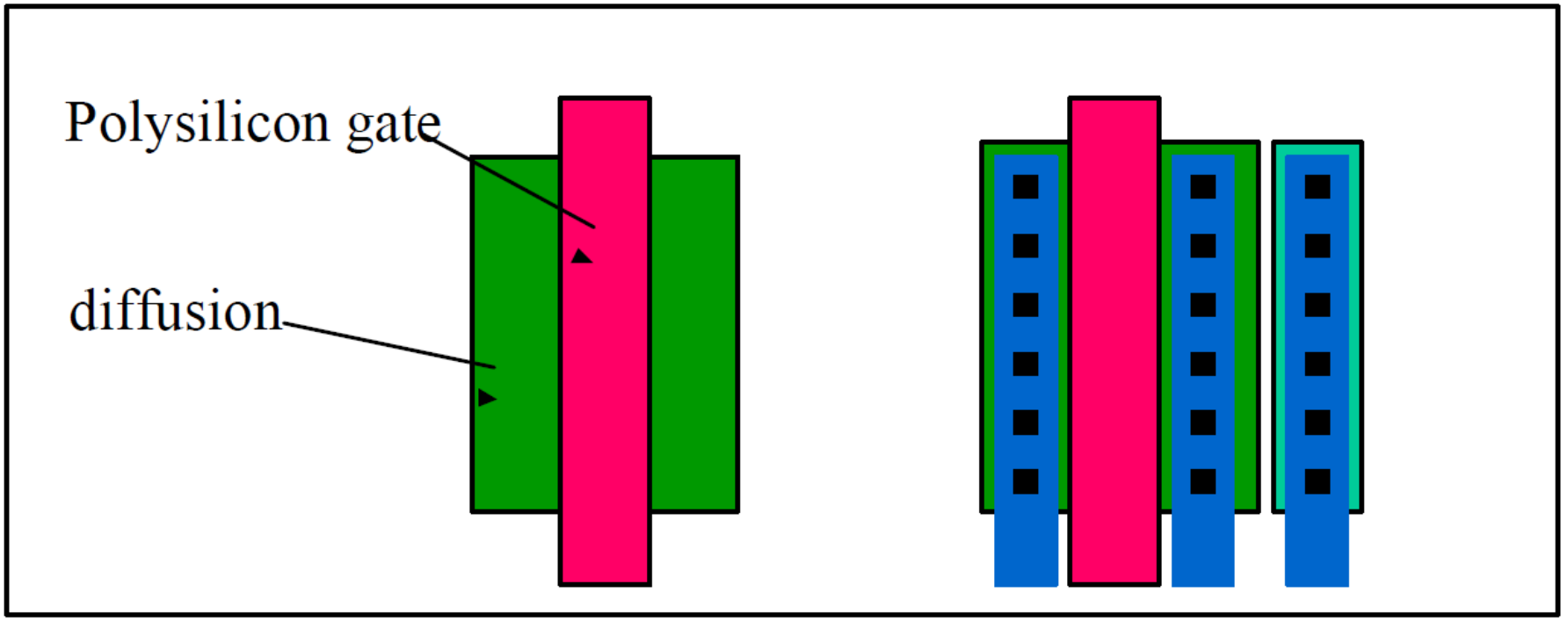
Lecture 3:

Basic Circuit Elements (MOSFET, Capacitor, Transistor)

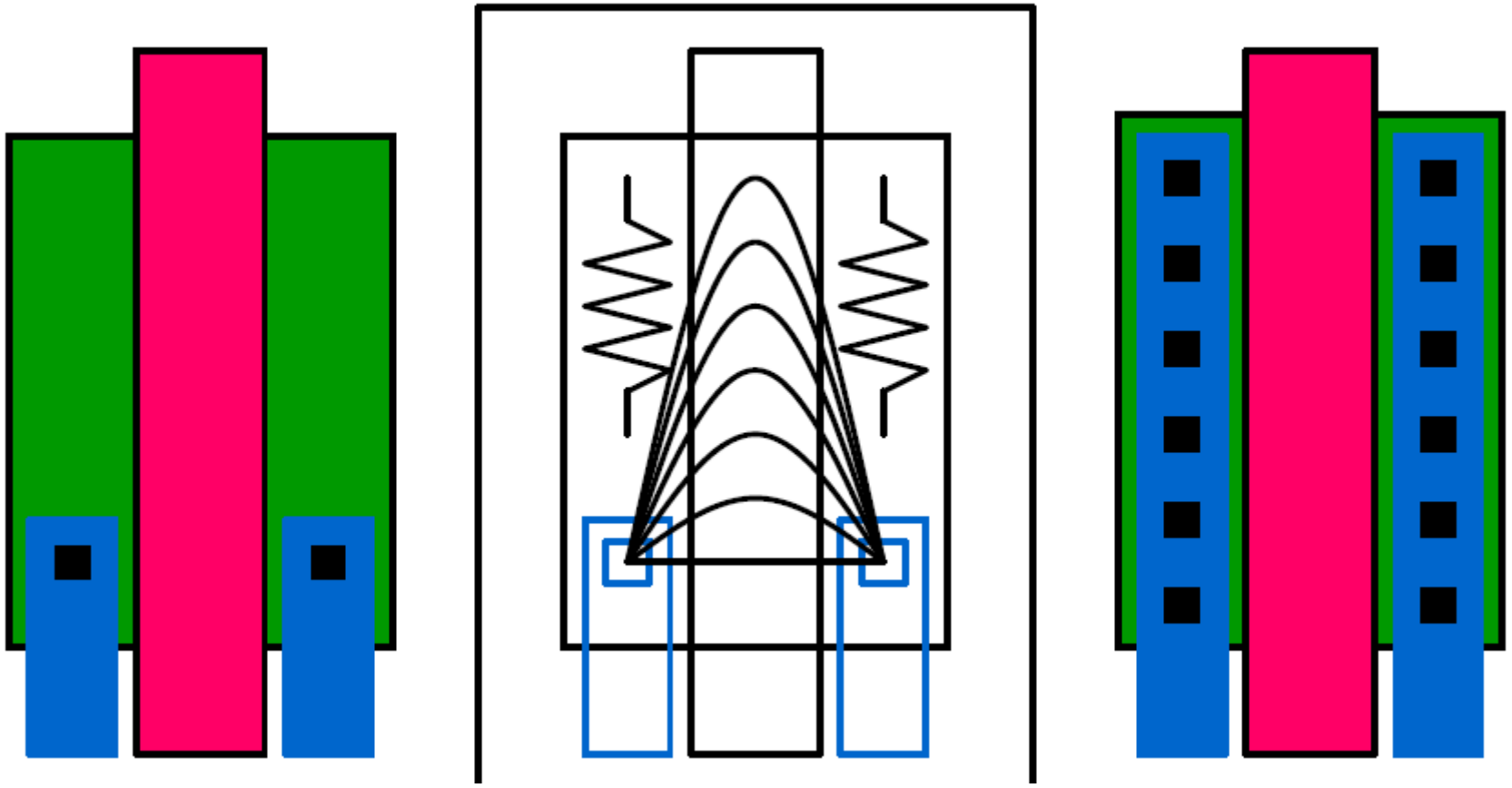
MOSFET

- A CMOS transistor is the crossing of two rectangles, polysilicon and active area.
- but, we need the drain and source connections and we need to bias the substrate or the well.



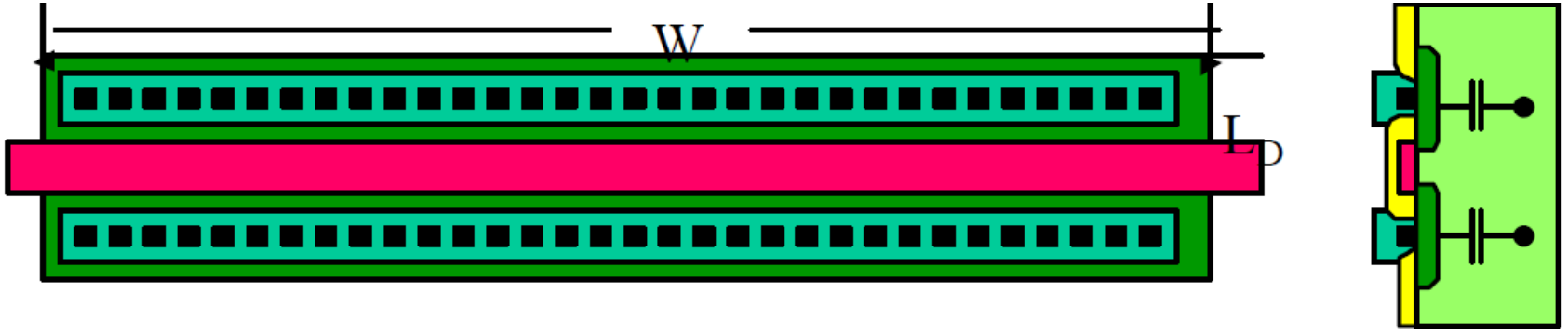
MOSFET

- Ensure good connections.



MOSFET

- Analog transistors often have a large W/L ratio.



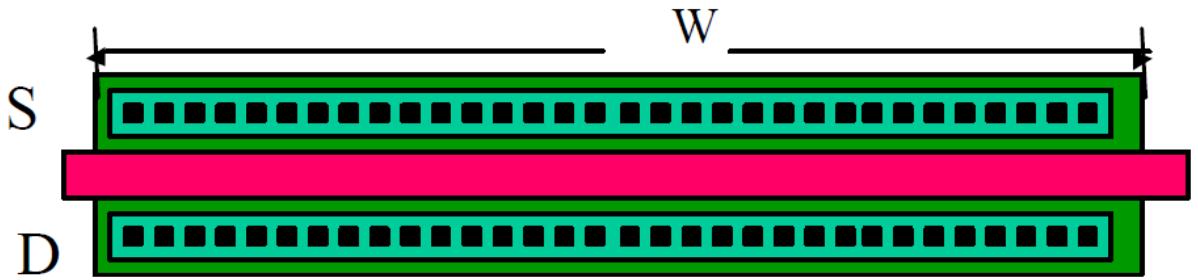
- Capacitance diffusion substrate.

$$C_{SB} = C_{DB} = (W + 2l_{diff})(L_D + 2l_{diff})$$

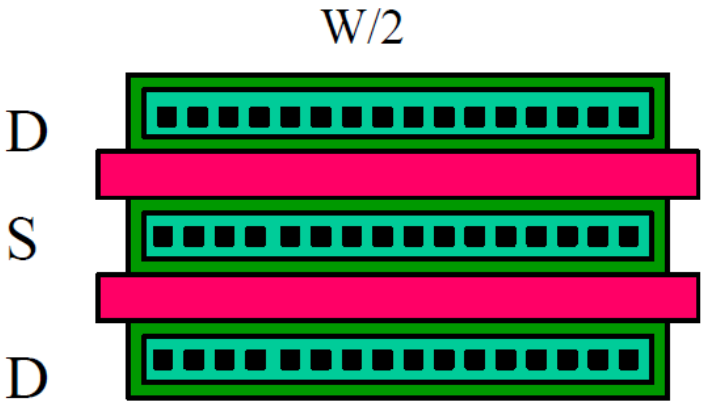
- Resistance of the poly gate.

$$R_{gate} = L_{gate} R_{sq,poly}$$

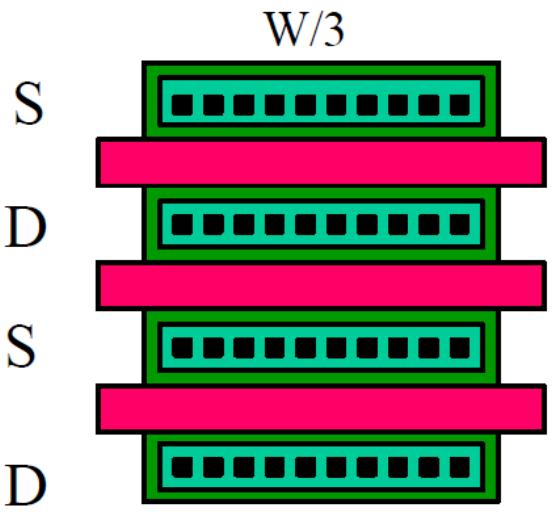
MOSFET



$$C'_{SB};C'_{DB}$$



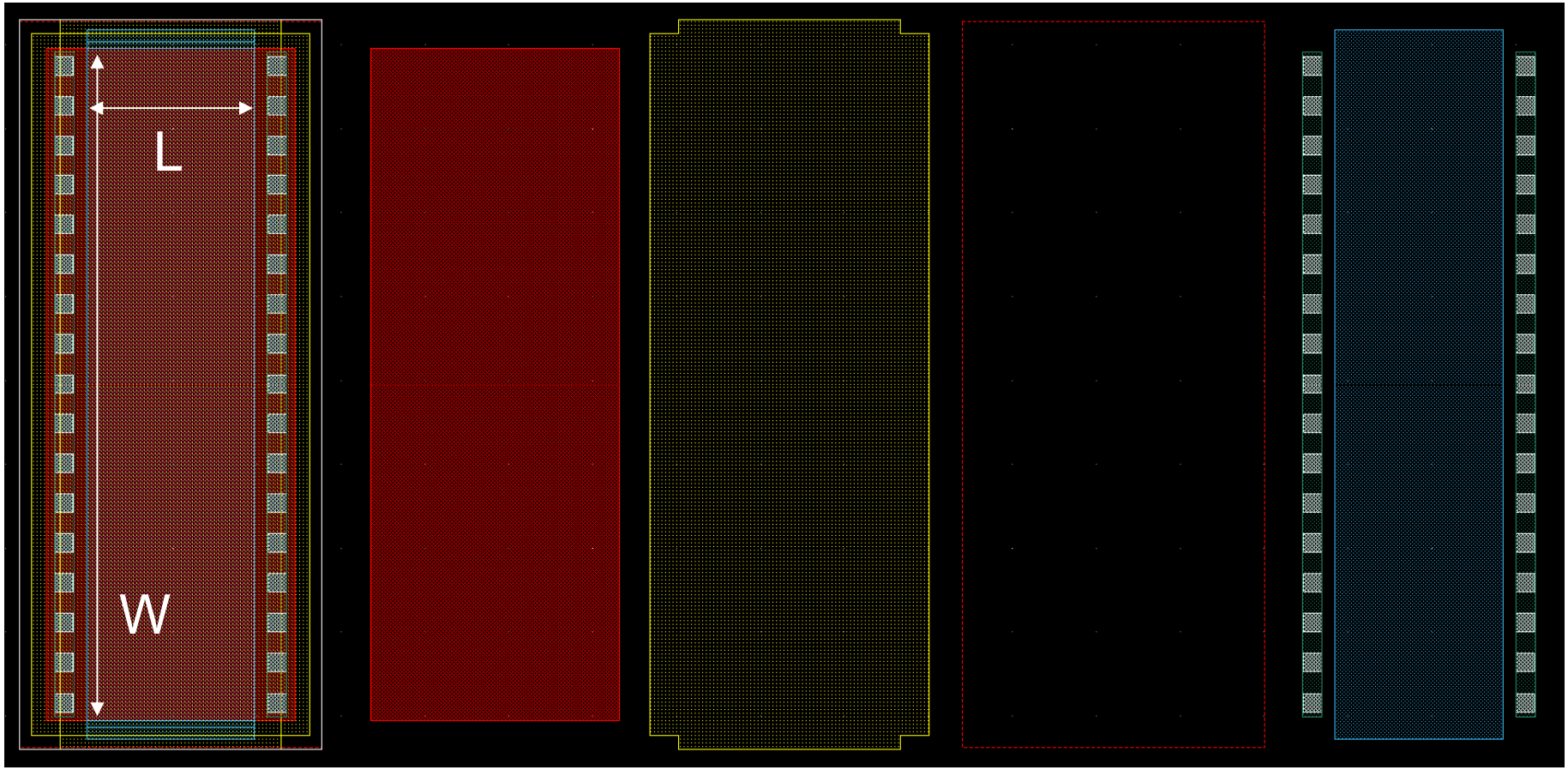
$$C_{SB}=\frac{1}{2}C_{DB};C_{DB}=C'_{DB}$$



$$C_{SB}=\frac{2}{3}C'_{SB}$$

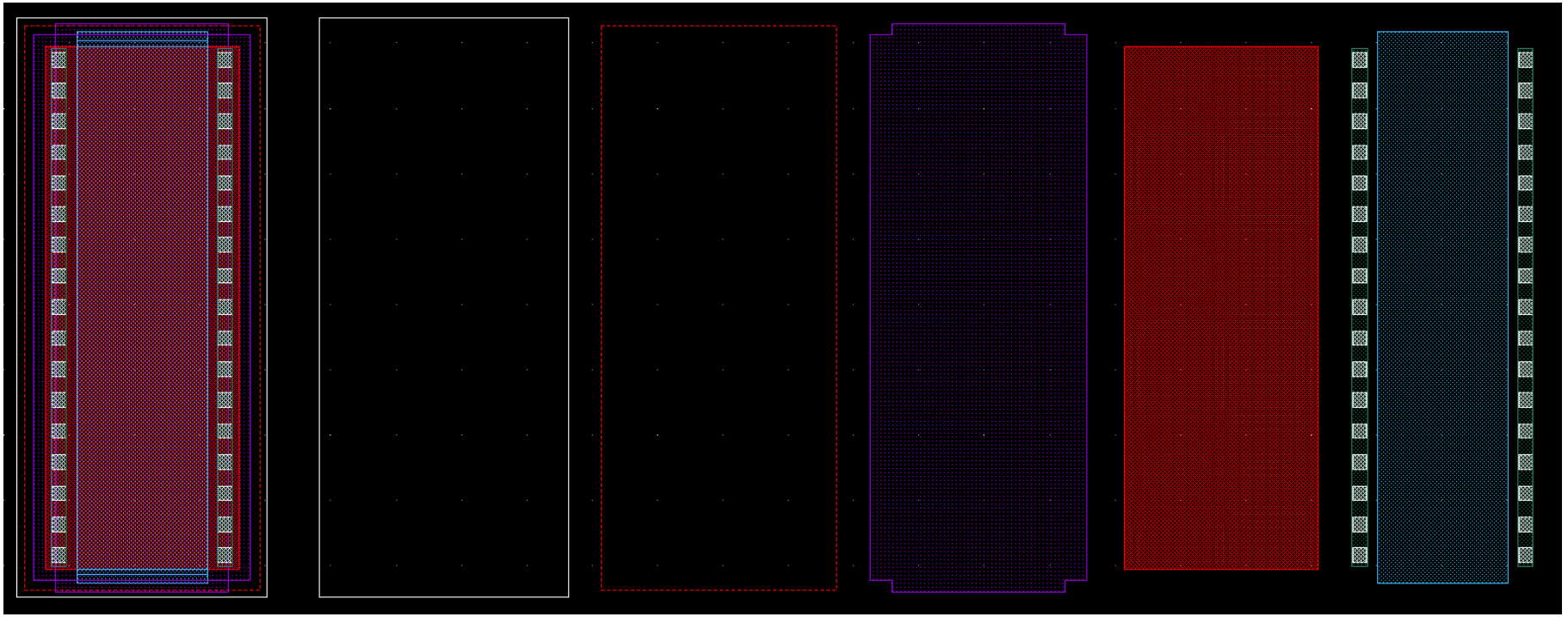
$$C_{DB}=\frac{2}{3}C'_{DB}$$

MOSFET



NCH3 ACT NPLUS TGO GATE, M1,CT

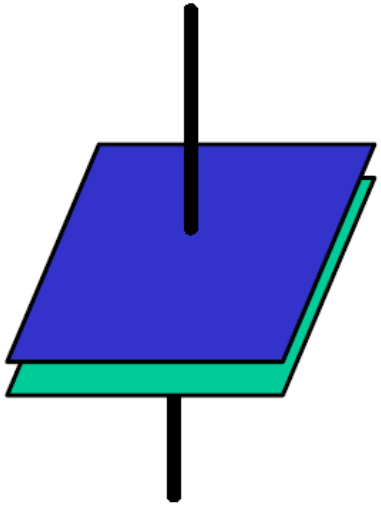
MOSFET



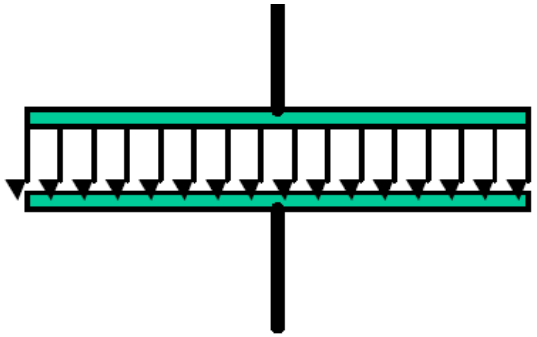
PCH3 NW TGO NPLUS ACT GATE, M1,CT

Capacitor

Capacitors in IC are parallel plate capacitors.



No fringing effect →



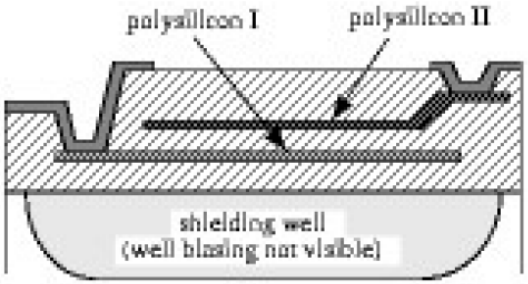
$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

Material	Rel. Permittivity	Diel. Strength
SiO_2 Dry Oxide	3.9	11 V/nm
SiO_2 Plasma	4.9	3-6 V/nm
Si_3N_4 LPCVD	6-7	10 V/nm
Si_3N_4 Plasma	6-9	5 V/nm

Capacitor

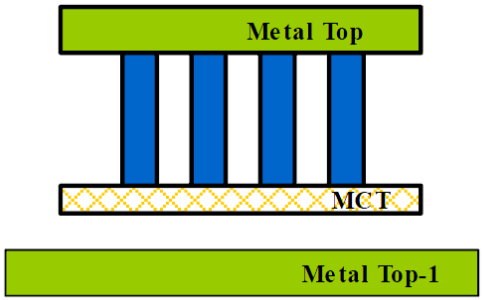
Types of integrated capacitors.

poly-poly

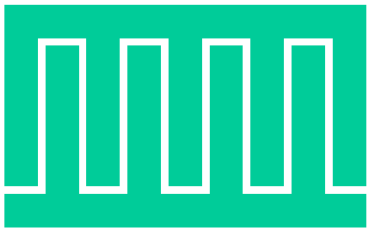


metal-metal(MIM)

Sandwich



Flux



Capacitor

Factor affecting accuracy

$\left(\frac{\Delta\varepsilon_r}{\varepsilon_r}\right)$

- Oxide damage
- Impurities
- Bias condition
- Bias history (for CVD)
- Stress
- Temperature

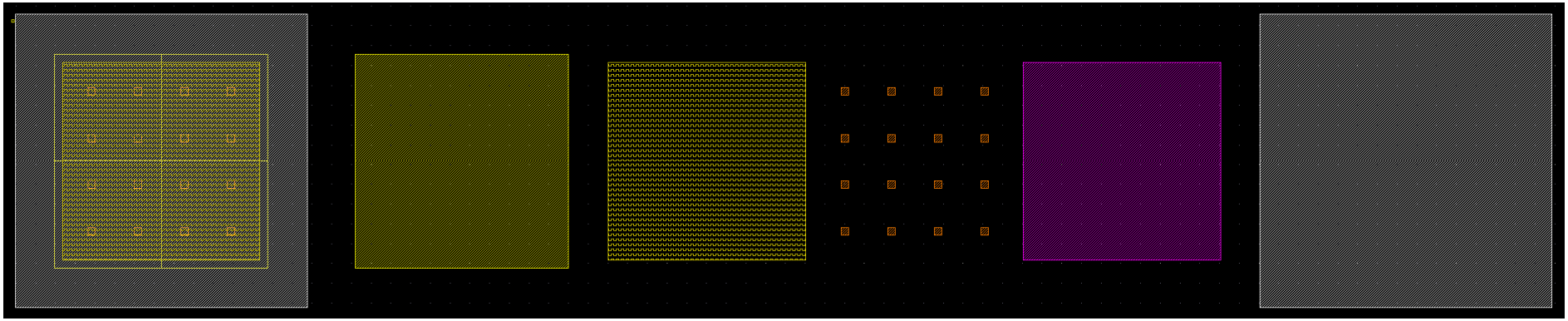
$\left(\frac{\Delta t_{ox}}{t_{ox}}\right)$

- Grow rate
- Poly grain size

$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$

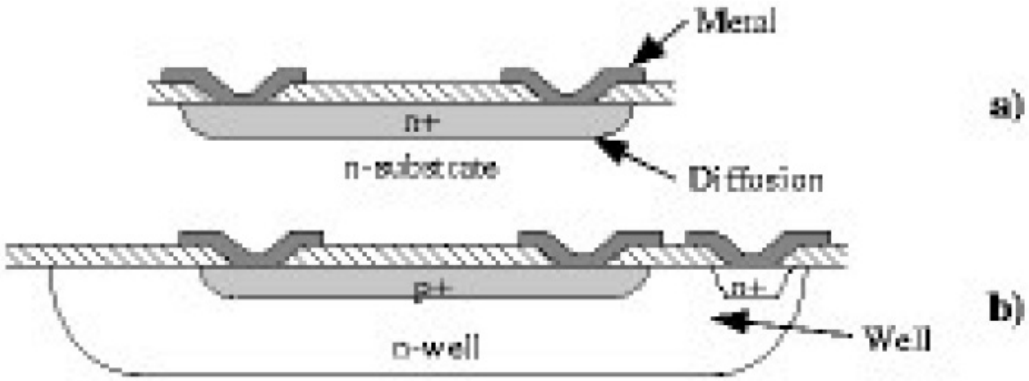
- Etching
- Alignment

Capacitor



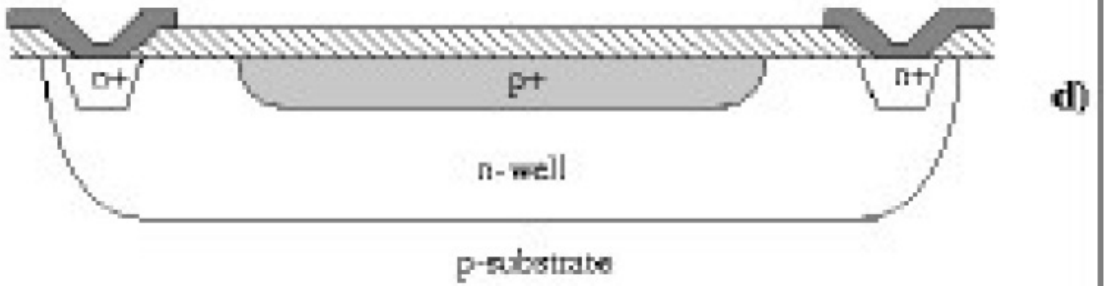
MIM_CAP M3 MCT MV3 M4 DUM_MCT

Transistor



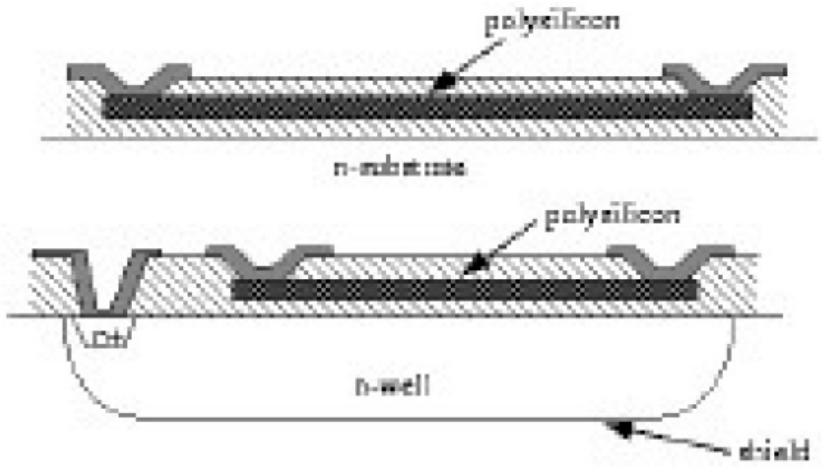
a,b) diffusion

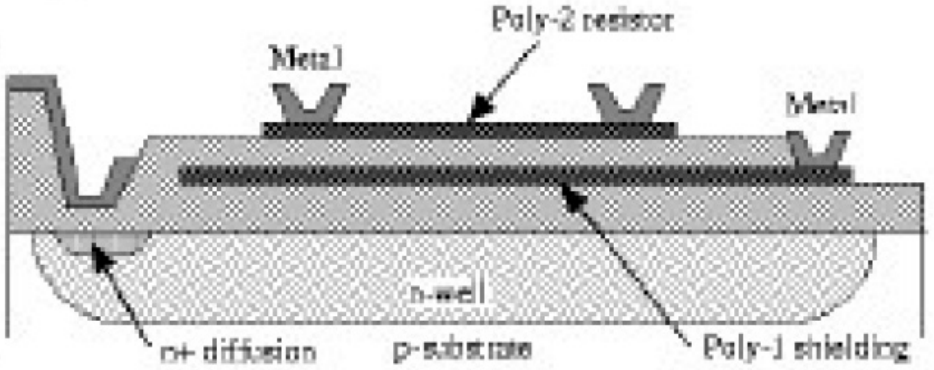
c) n-well (or p-well)



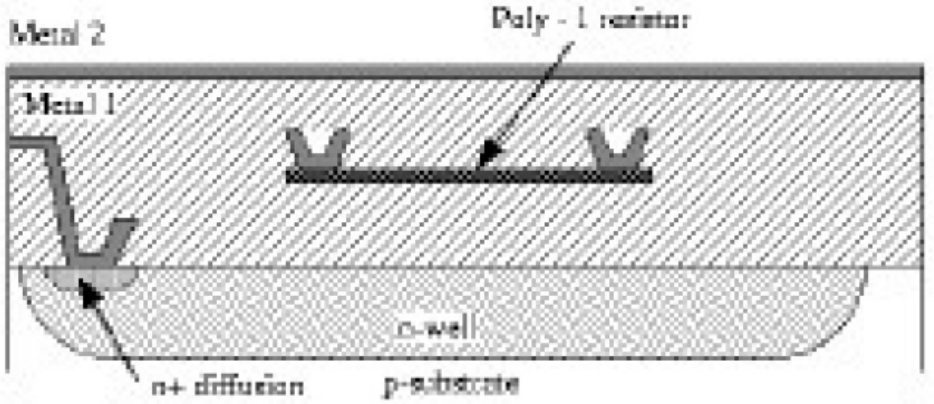
d) Pinched well

Transistor

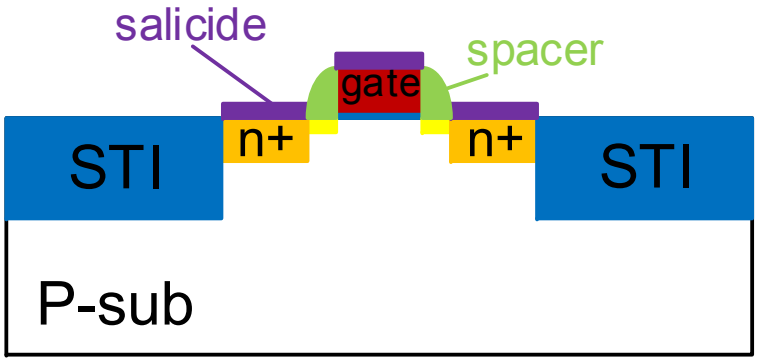


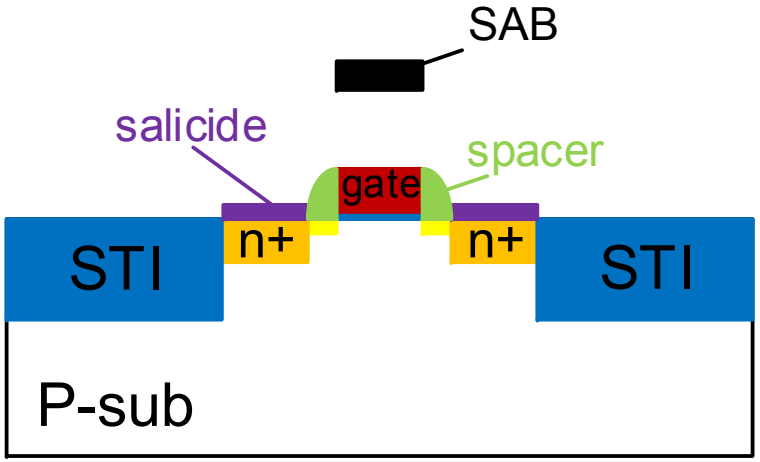


Conductive layers can be used to shield the conductor-oxide-conductor structure

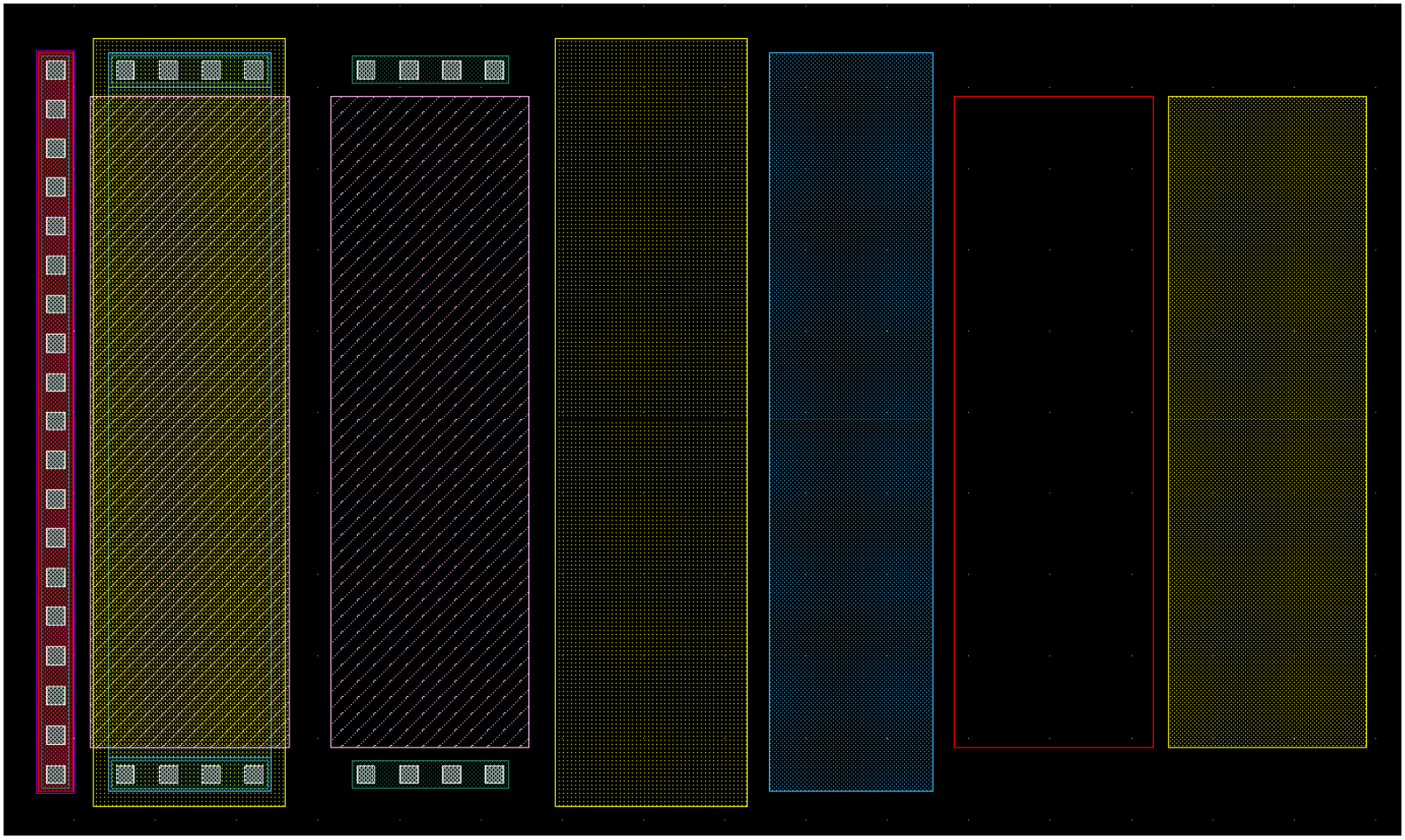


Transistor


salicide
spacer
gate
STI
n+
n+
STI
P-sub


SAB
salicide
spacer
gate
STI
n+
n+
STI
P-sub

Transistor



RNPOLYU3

NPLUS

SAB

DUM_RM

GATE

RNDMY

Computer Lab

1. Draw a NCH3 and a PCH3 MOSFET.

   Total W/L=10um/0.5um, finger=5

2. Draw a RNPOLYU3 resistor. W/L=20um/2um

3. Draw a MIM_CAP capacitor. W/L=15um/15um

4. Complete the DRC and LVS verification of the above devices.

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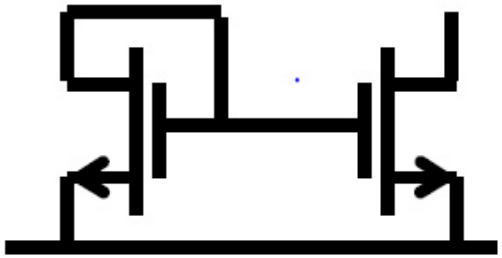
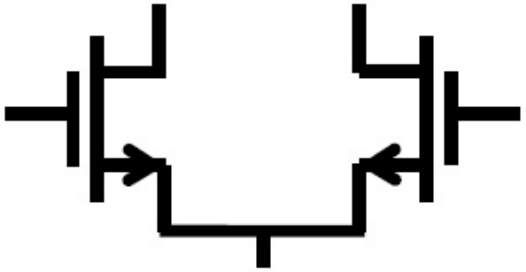
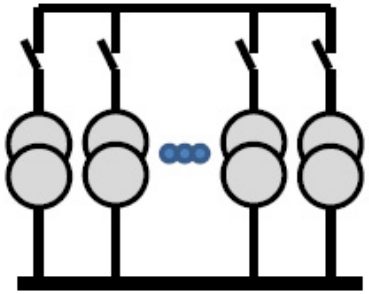
Lecture 4:

Matching

CMOS analog design relies on matching







Biasing

- PVT sensitivity
- Operating headroom
- Quiescent Control
- Safe Operating Area

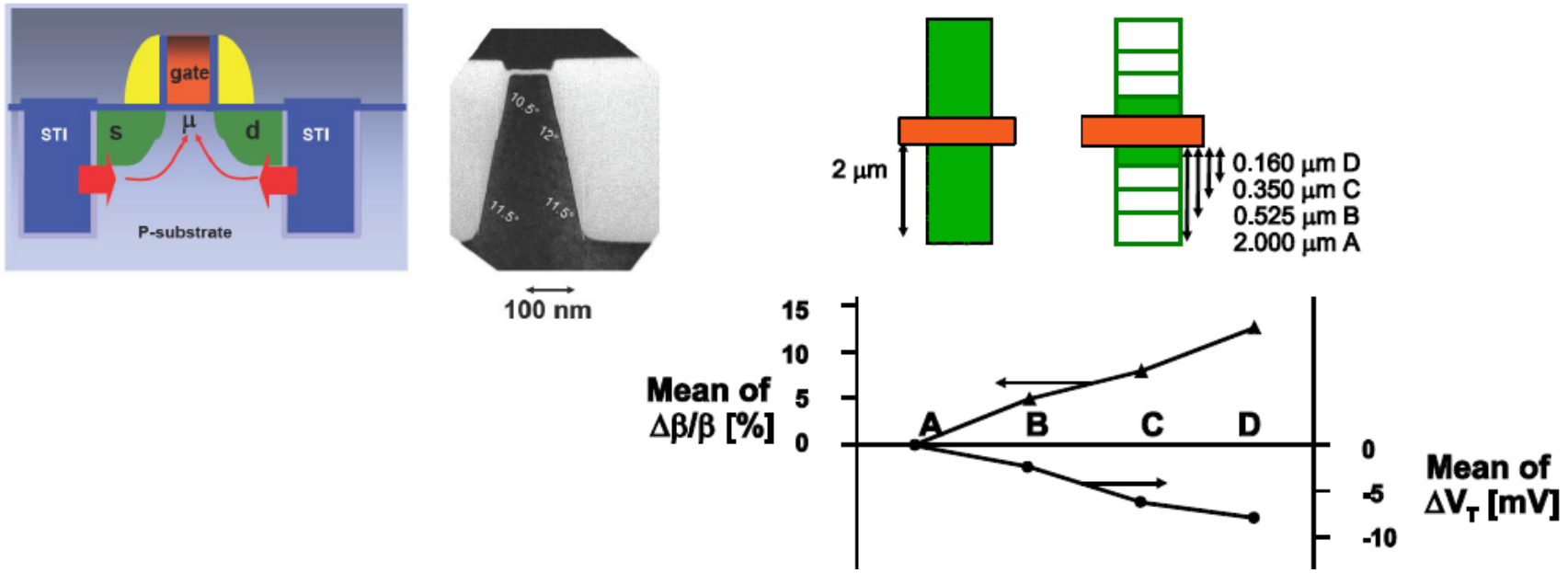
Offset

- Input pairs
- Common Mode
- Range
- CMRR
- PSRR

Precision

- Converter resolution
- INL
- DNL
- SFDR

Non-ideal factors: STI stress



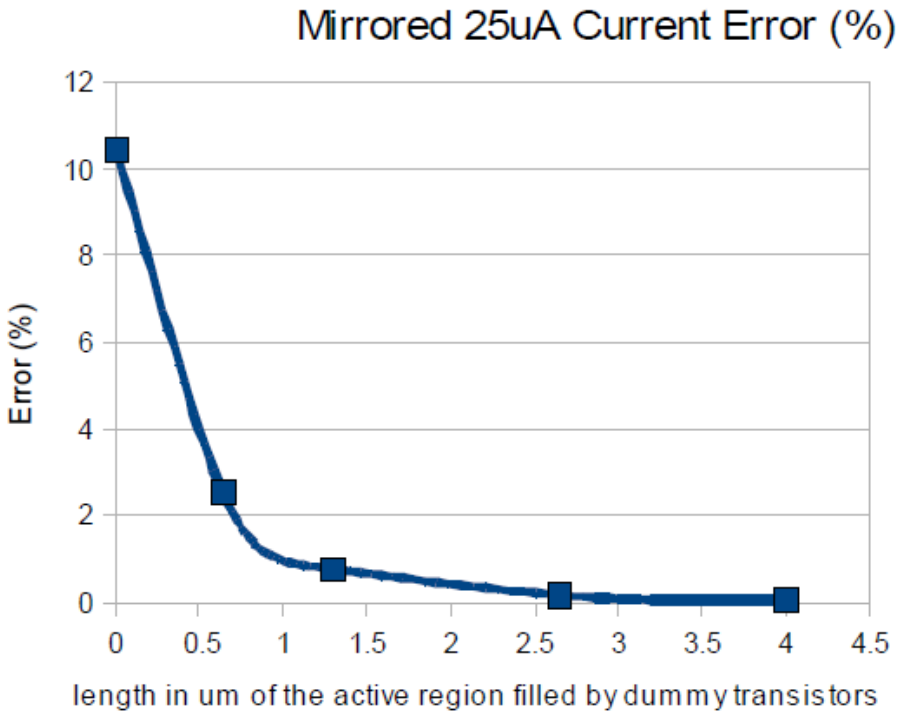
Can have a huge effect – up to 20% gm

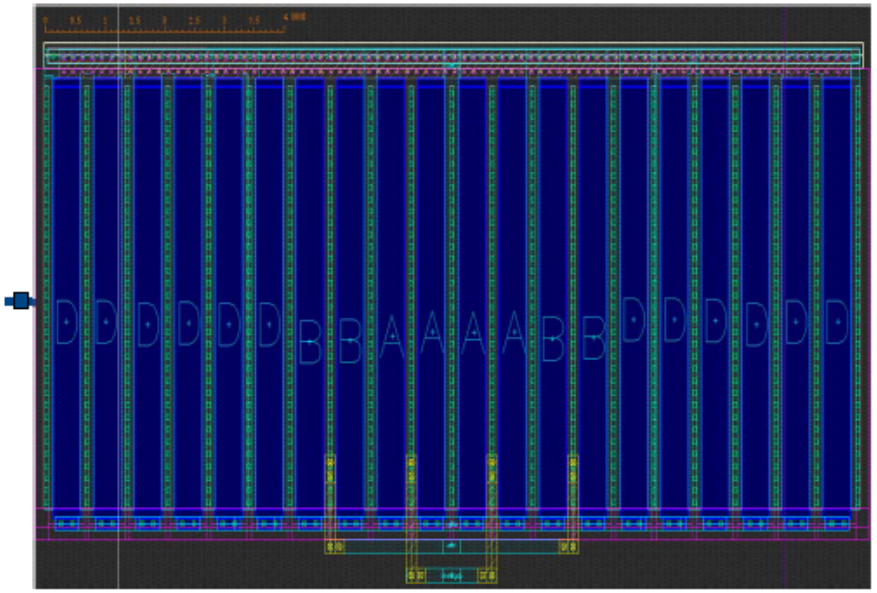
Can be extracted so

i) don't leave it to the end of the design/layout cycle to check

ii) Make it part of the design flow, i.e. should check layout meets design

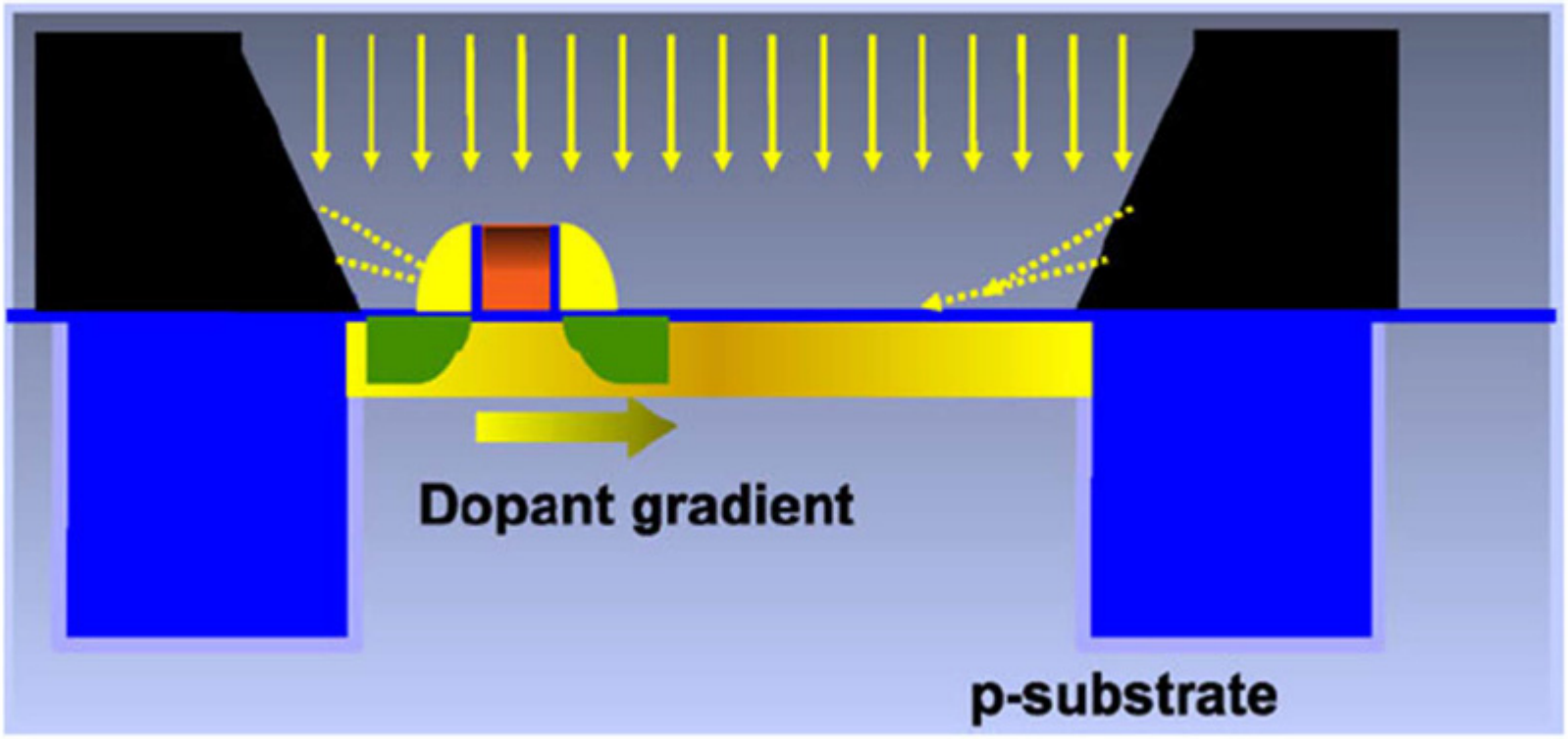
Non-ideal factors: STI stress





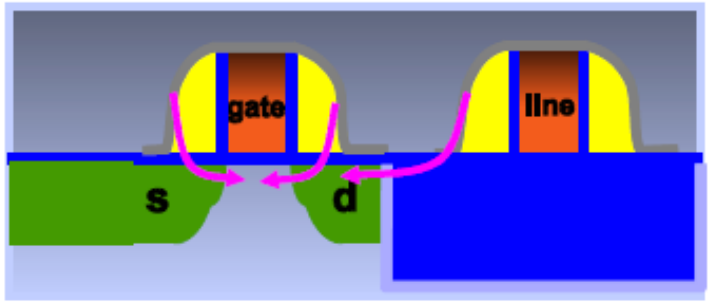
Yes/No - this study shows 4um of dummy transistors are needed to minimize the effects of STI.

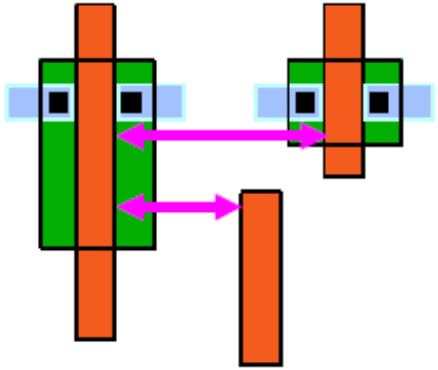
Non-ideal factors: Well proximity effects

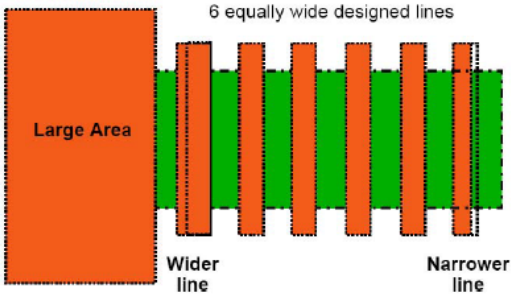


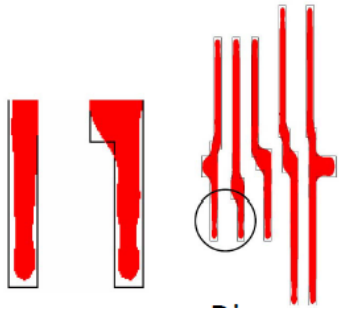
Transistors close to the well edge will exhibit a difference in Vt and Id compared to devices located far away from well edge.

Non-ideal factors: Poly proximity effects





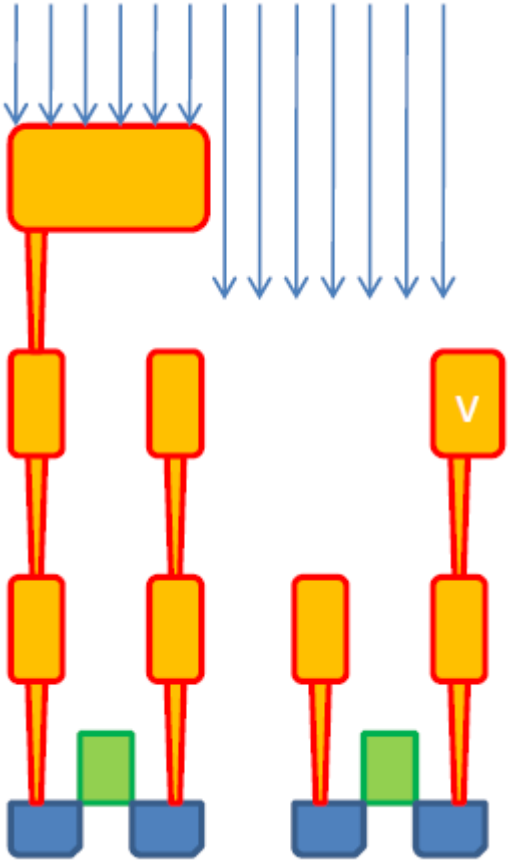




Poly Near transistors can

- Induce strain
- Influence etch uniformity
- Alter lithography

Non-ideal factors: Metal over transistor

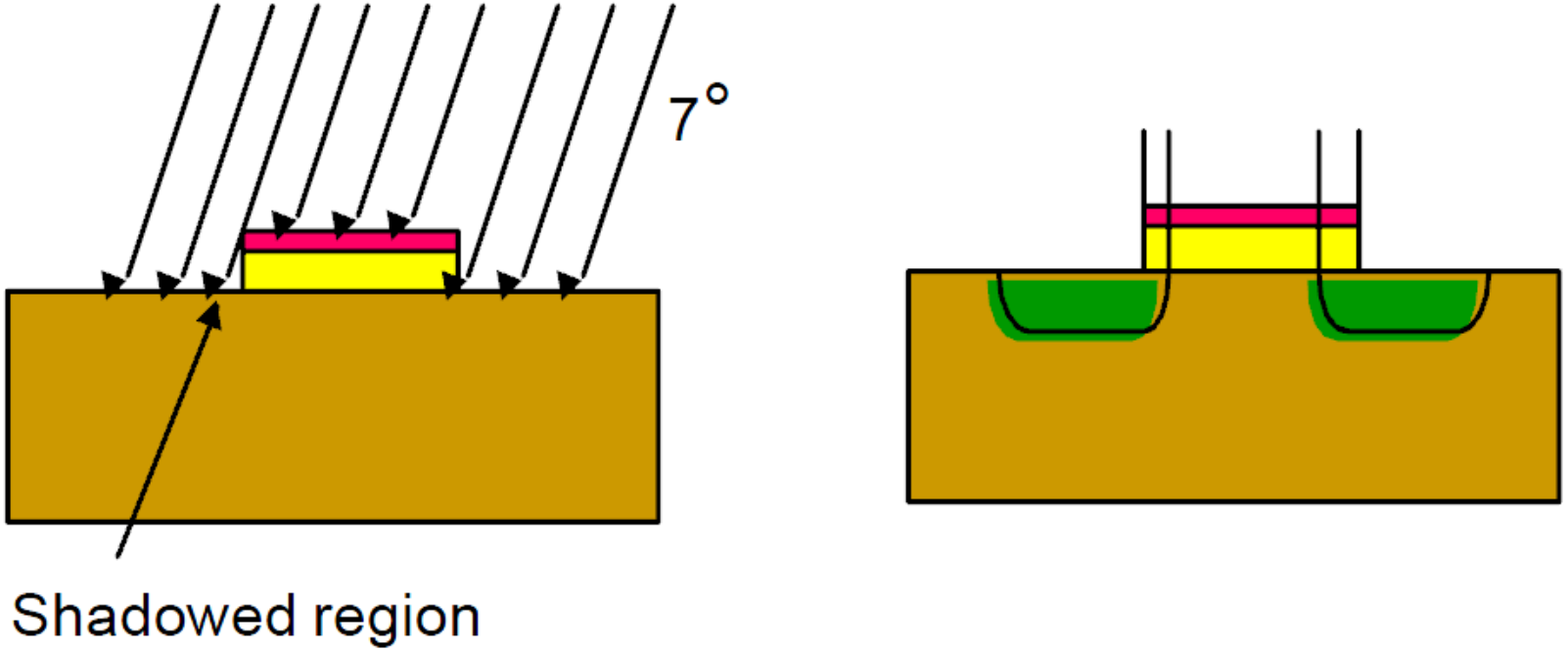


Hydrogen released at final process anneal can be blocked by the metal.

Metal over transistor can
– Prevent annealing
– Introduce stress

Non-ideal factors: Asymmetry

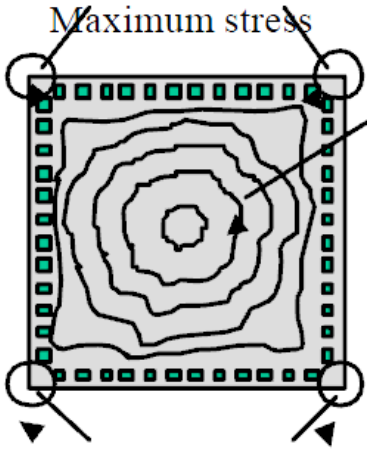
An MOS transistor is not a symmetrical device. To avoid channeling of implanted ions the wafer is tilted by about 7°.

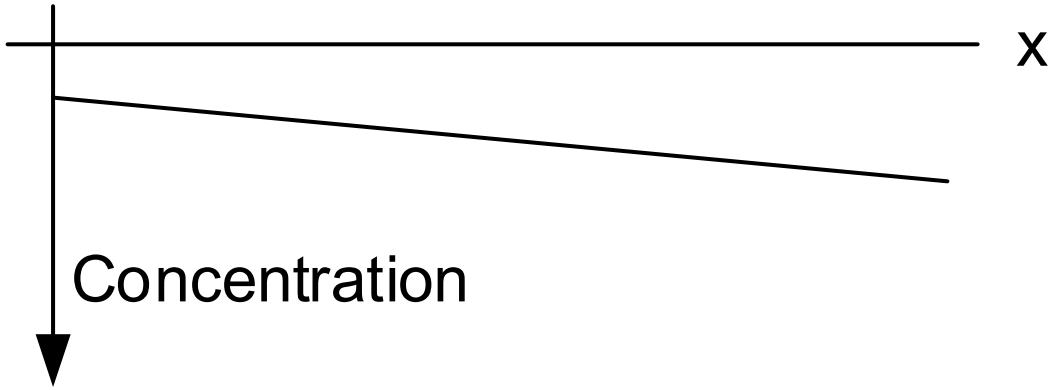


Source and drain are not equivalent

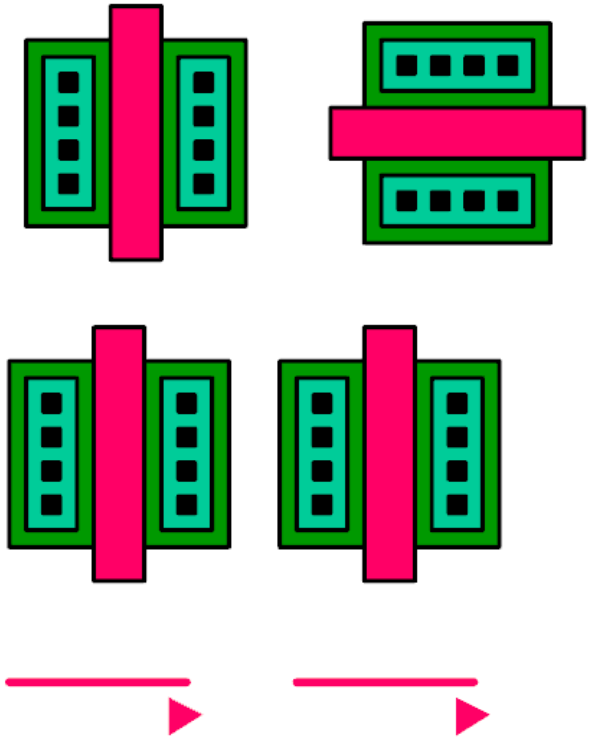
Non-ideal factors: Gradients

The effect of thermal or process linear gradients may be present in an integrated circuit, which can change the electrical characteristics of a device.

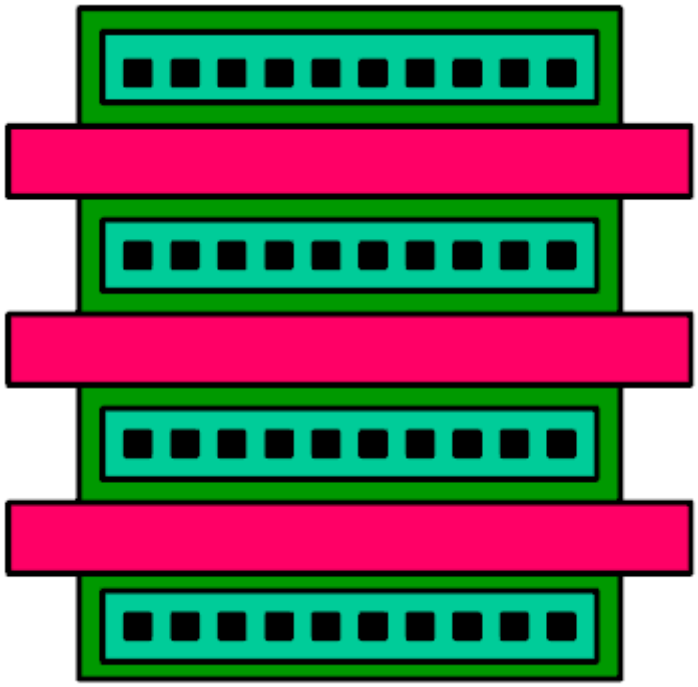




Matching single transistors



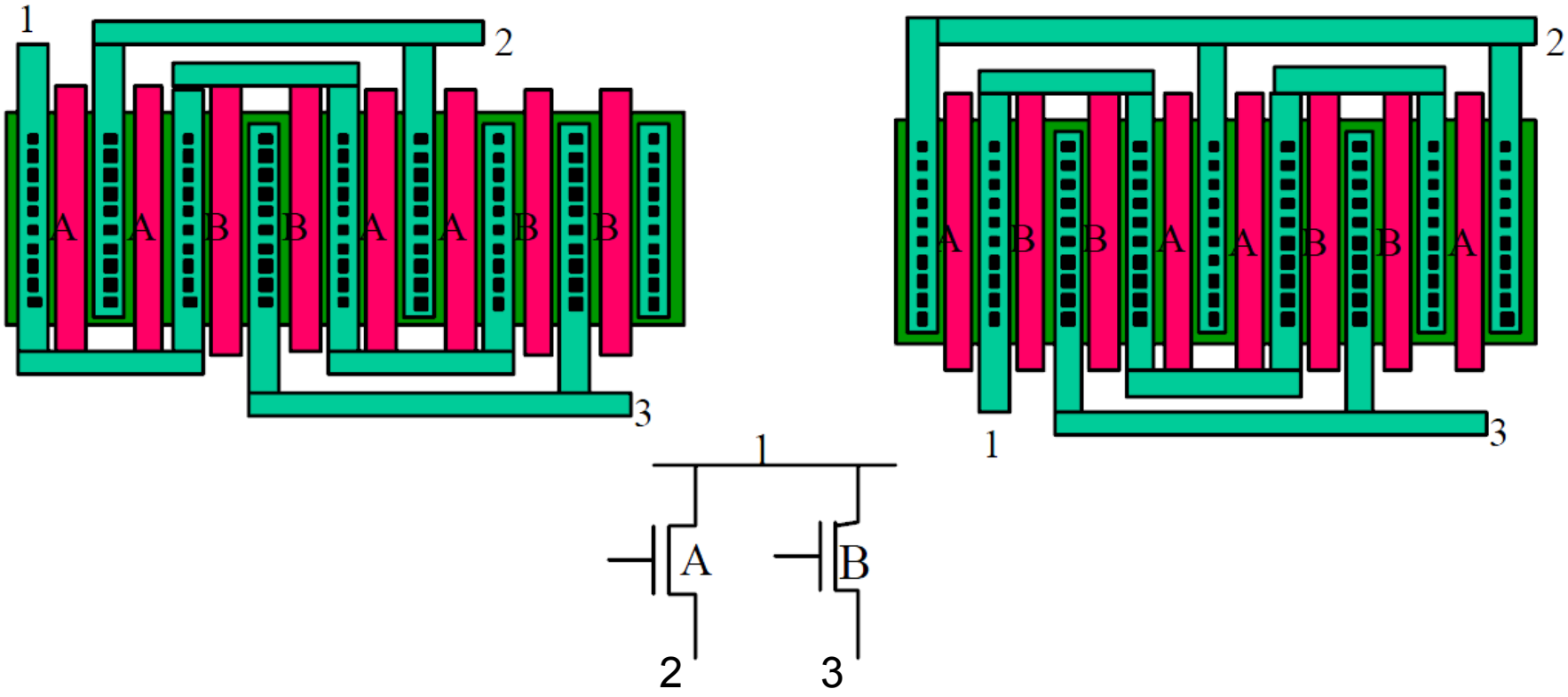
the current flowing
in the same direction



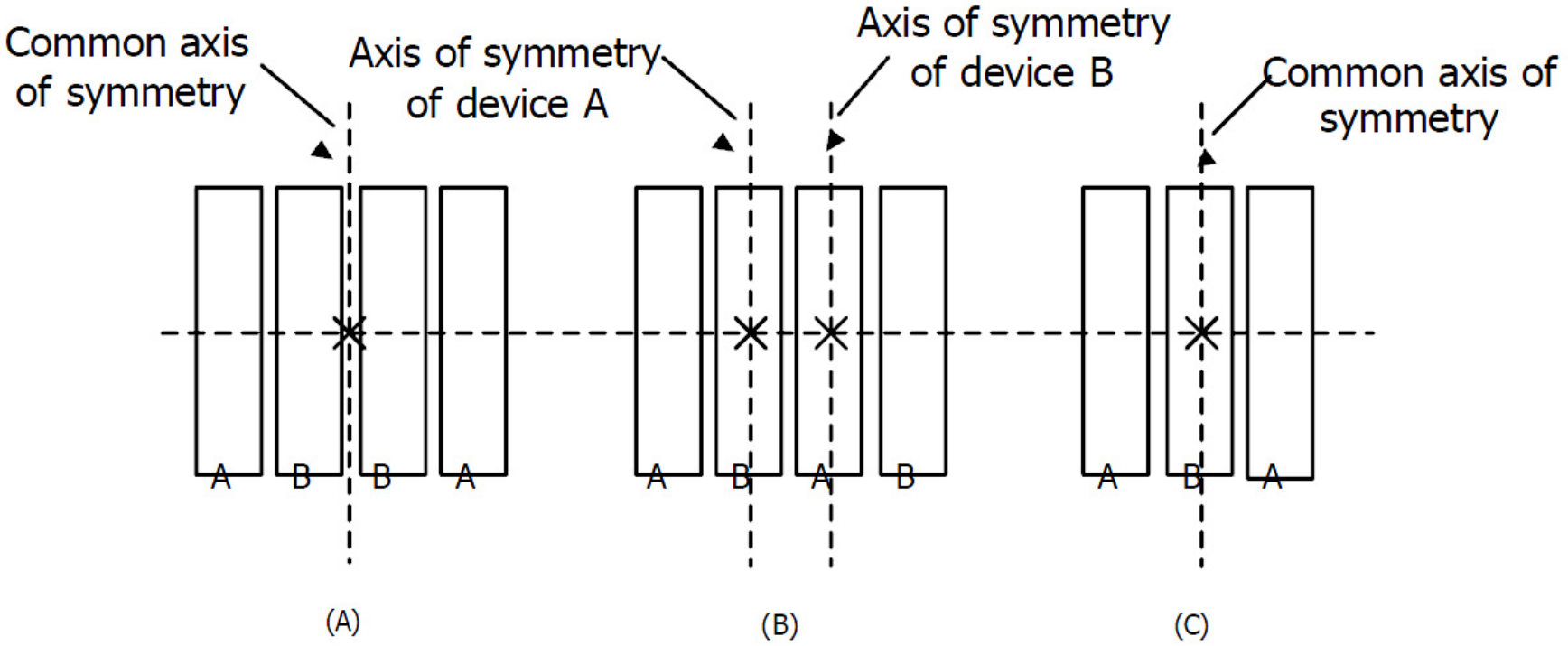
Use of multiple fingers

Interdigitated Devices

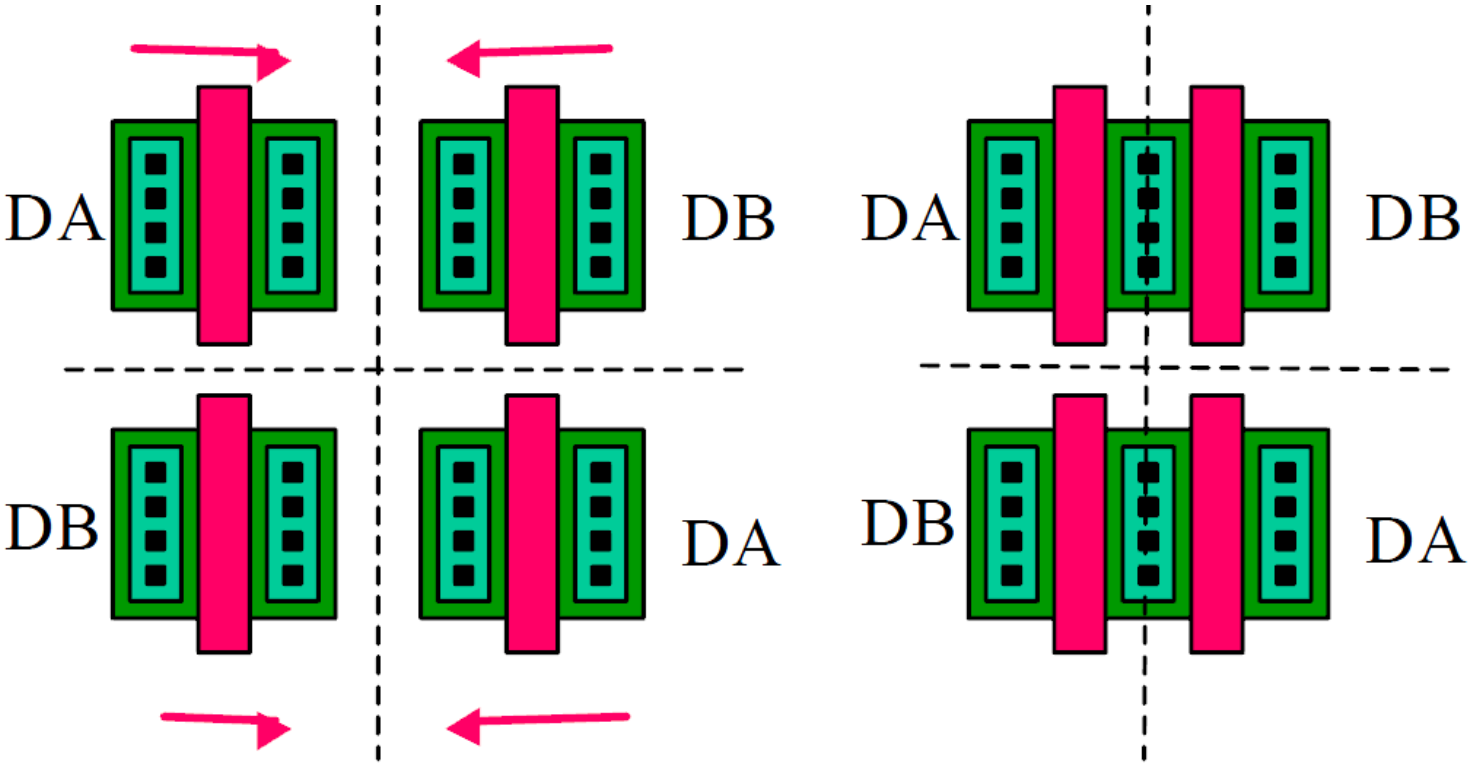
- Two matched transistors with one node in common
- spilt them in an equal part of fingers (for example 4)
- interdigitate the 8 elements: AABBAABB or ABBAABBA



Axis of symmetries

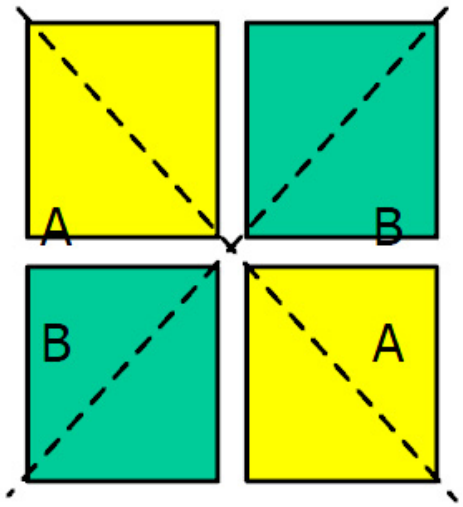


Common Centroid

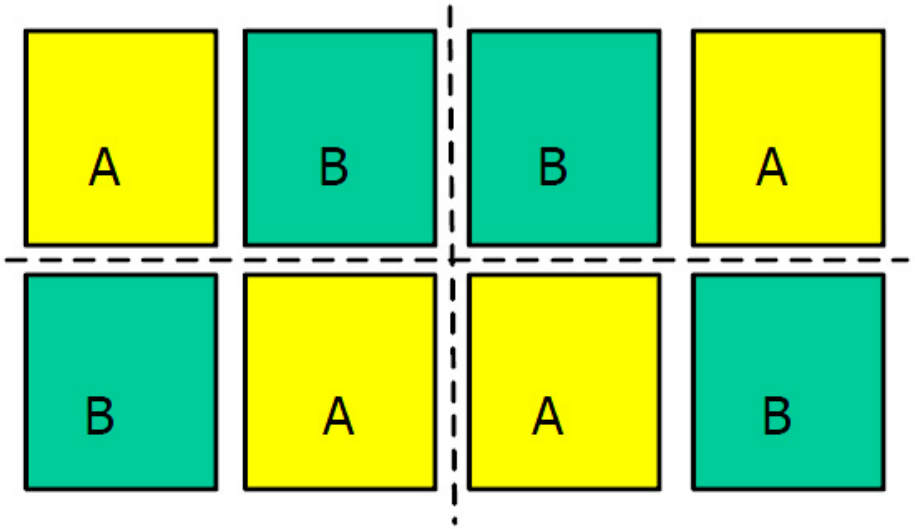


- Gradients in features are .
- metal and poly interconnections are more complex

Common Centroid Arrays



Cross coupling



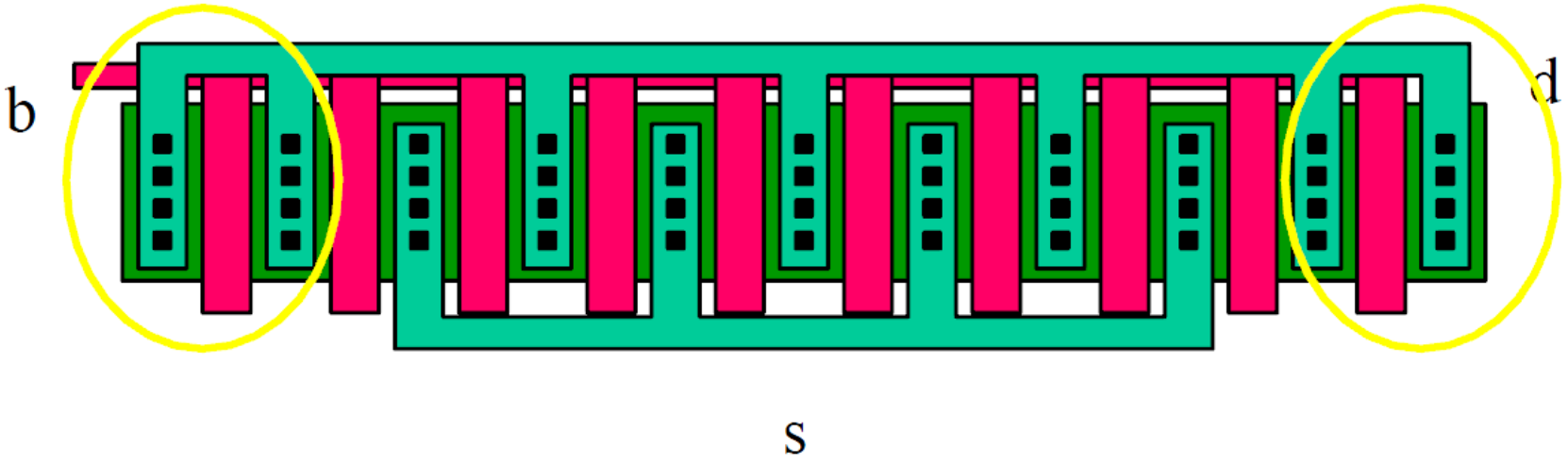
Tiling (more sensitive to high-order gradients)

Common Centroid Patterns

ABBA BAAB	ABBAABBA BAABBAAB	ABBAABBA BAABBAAB ABBAABBA	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
ABA BAB	ABAABA BABBAB	ABAABA BABBAB ABAABA	ABAABAABA BABBABBAB BABBABBAB ABAABAABA
ABCCBA CBAABC	ABCCBAABC CBAABCCBA	ABCCBAABC CBAABCCBA ABCCBAABC	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
AAB BAA	AABBAA BAAAAB	AABBAA BAAAAB AABBAA	AABBAA BAAAAB BAAAAB AABBAA

Dummy Devices on Ends

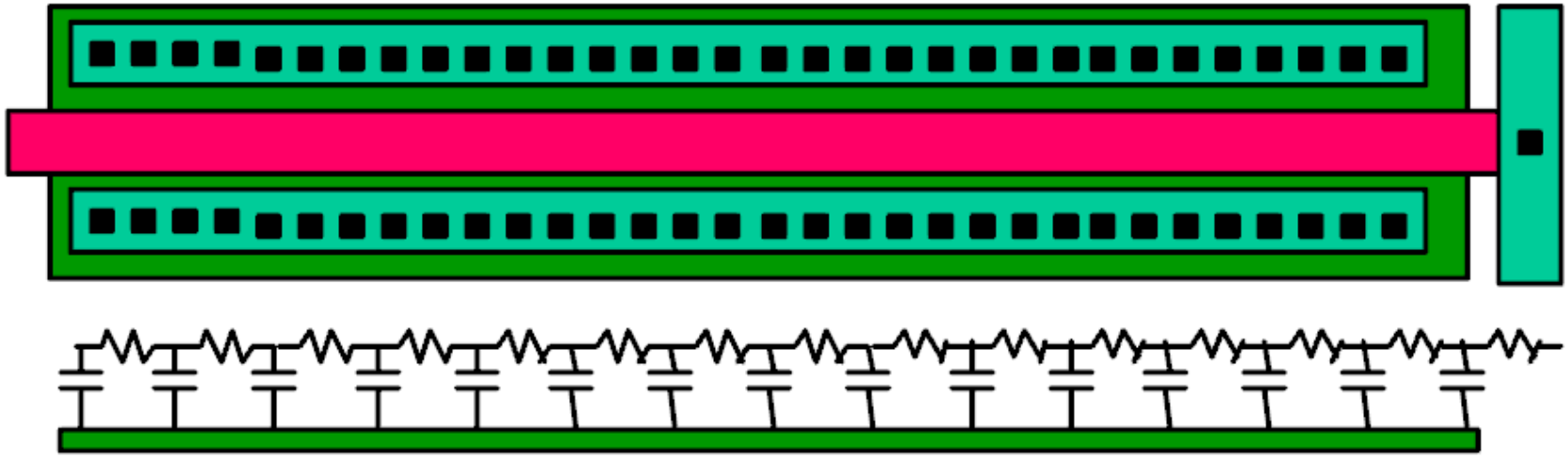
- Ending elements have different boundary conditions than the inner elements -> use dummy



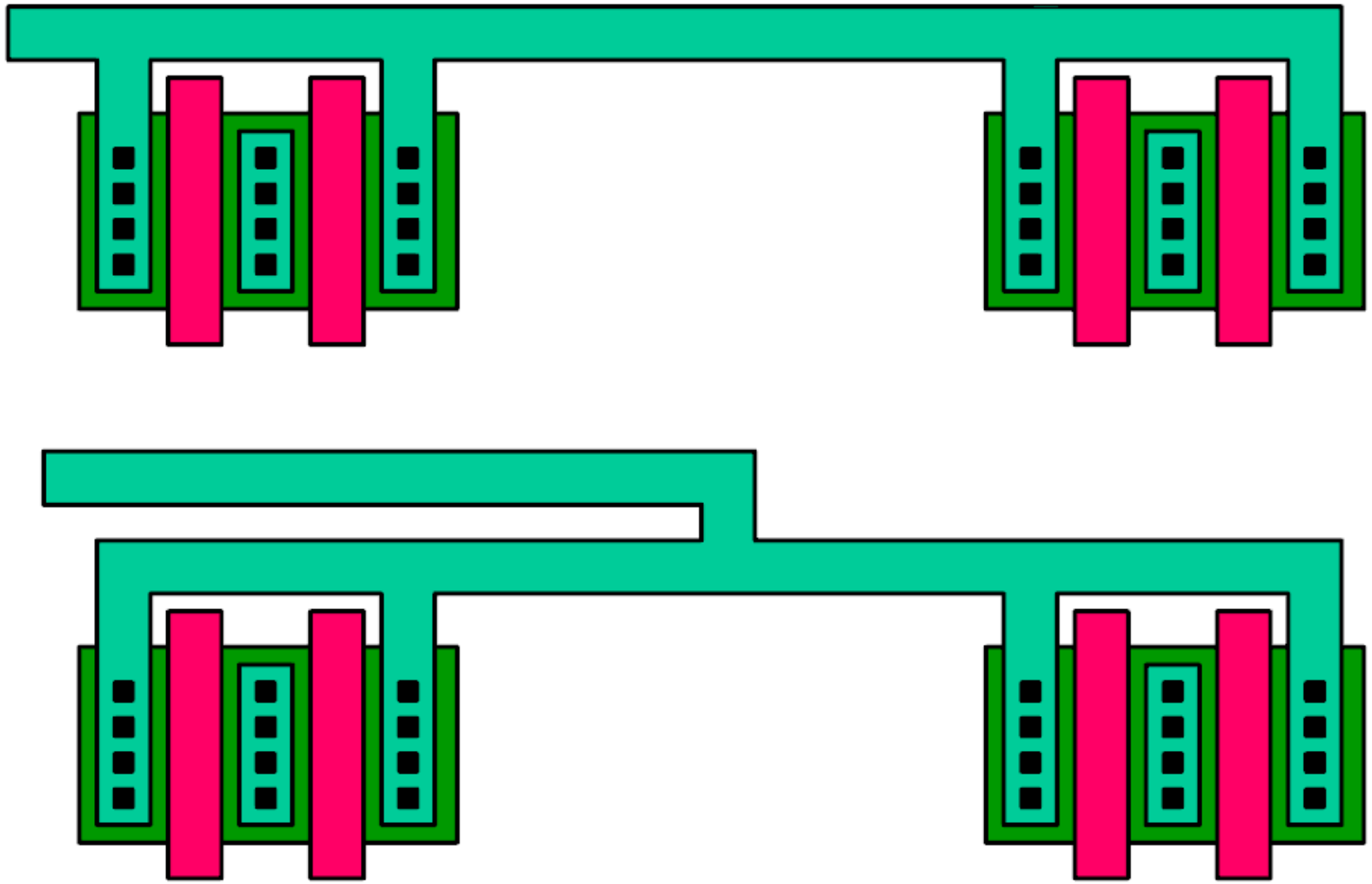
- Dummies are shorted transistors
- Remember their parasitic contribution!

Matched interconnections

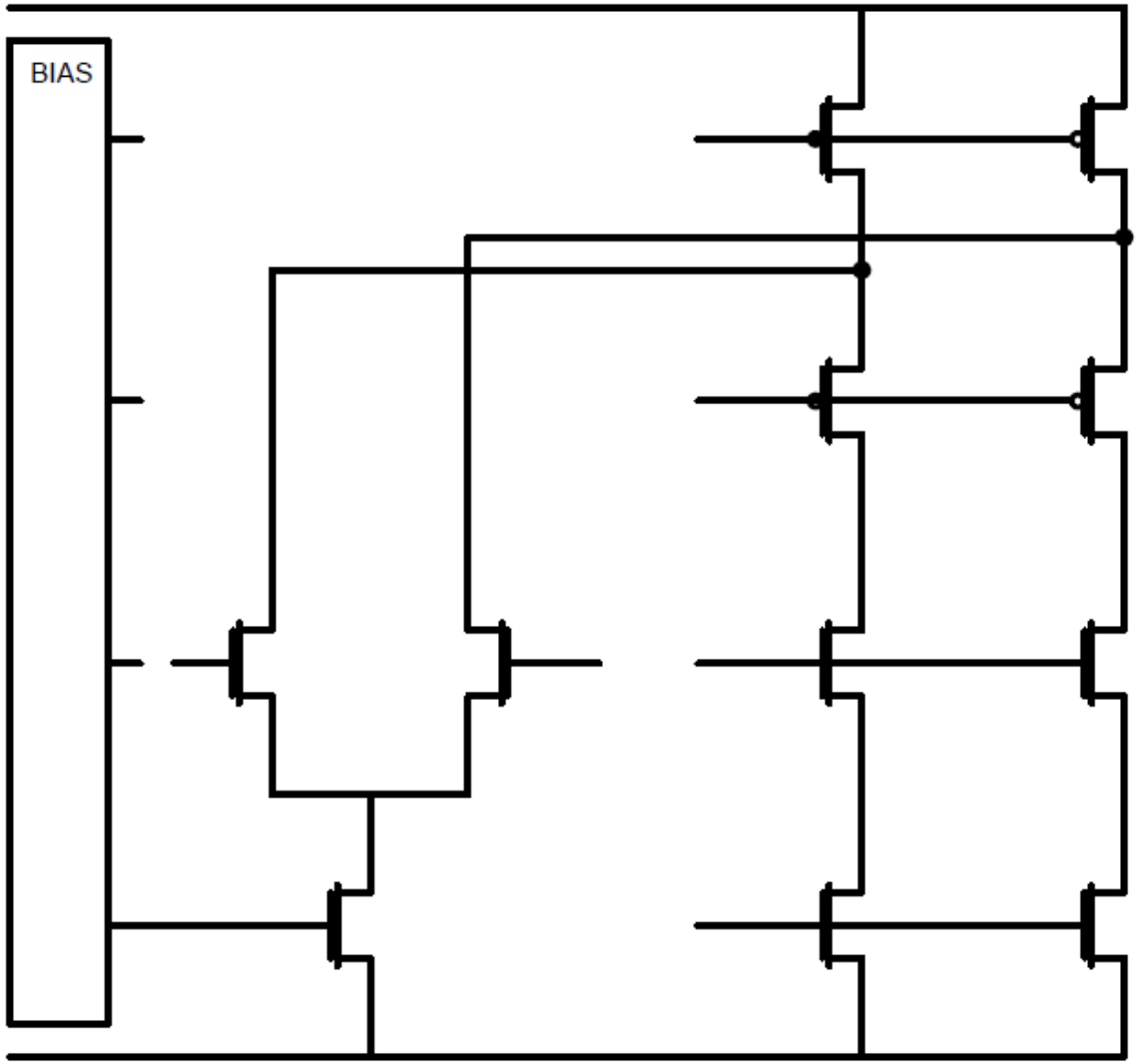
- Specific resistance of metal lines
- Specific resistance of poly
- Resistance of metal-contact
- Resistance of via
- Minimize the interconnection impedance
- Achieve the same impedance in differential paths



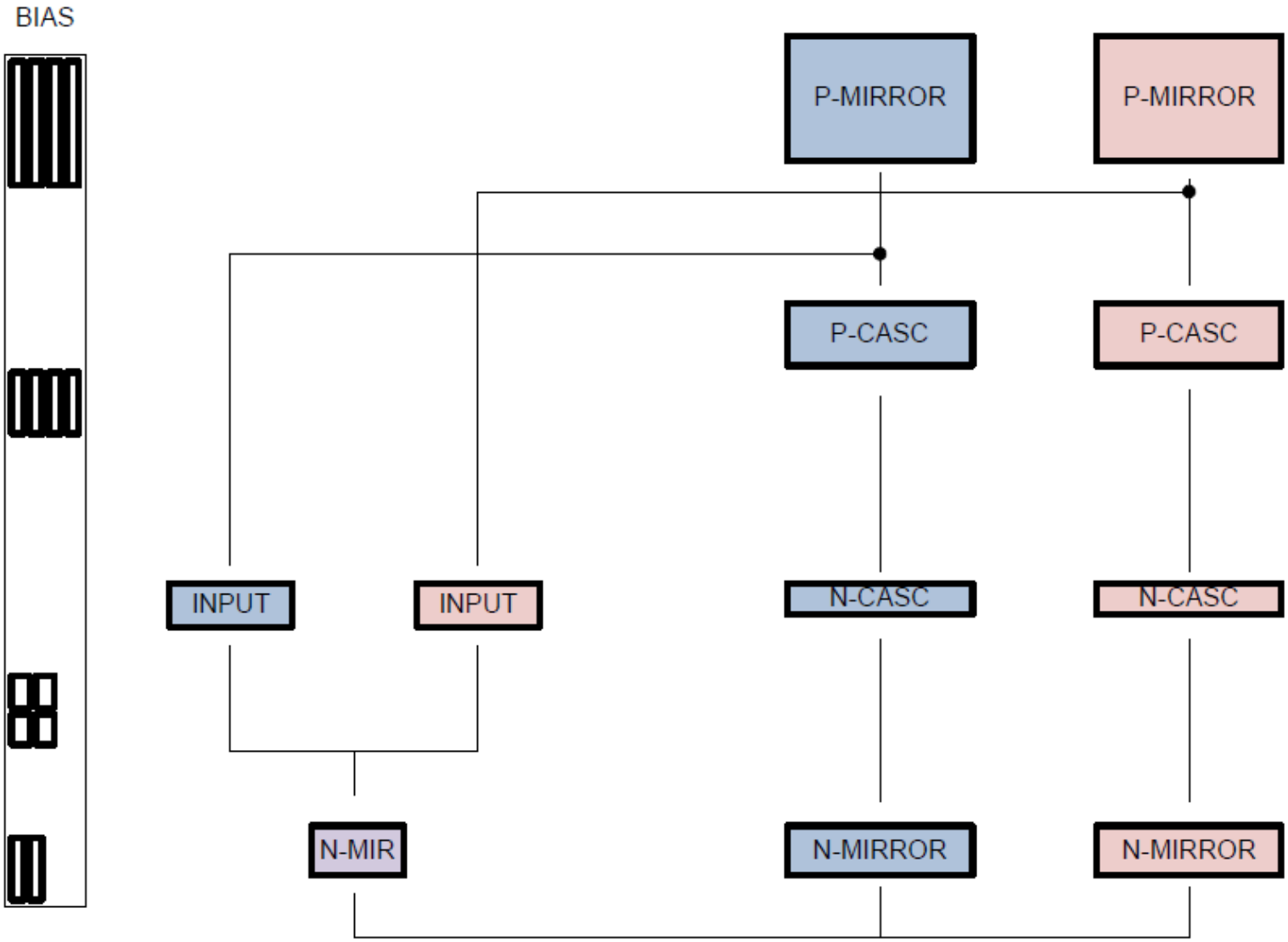
Matched Metal Connection



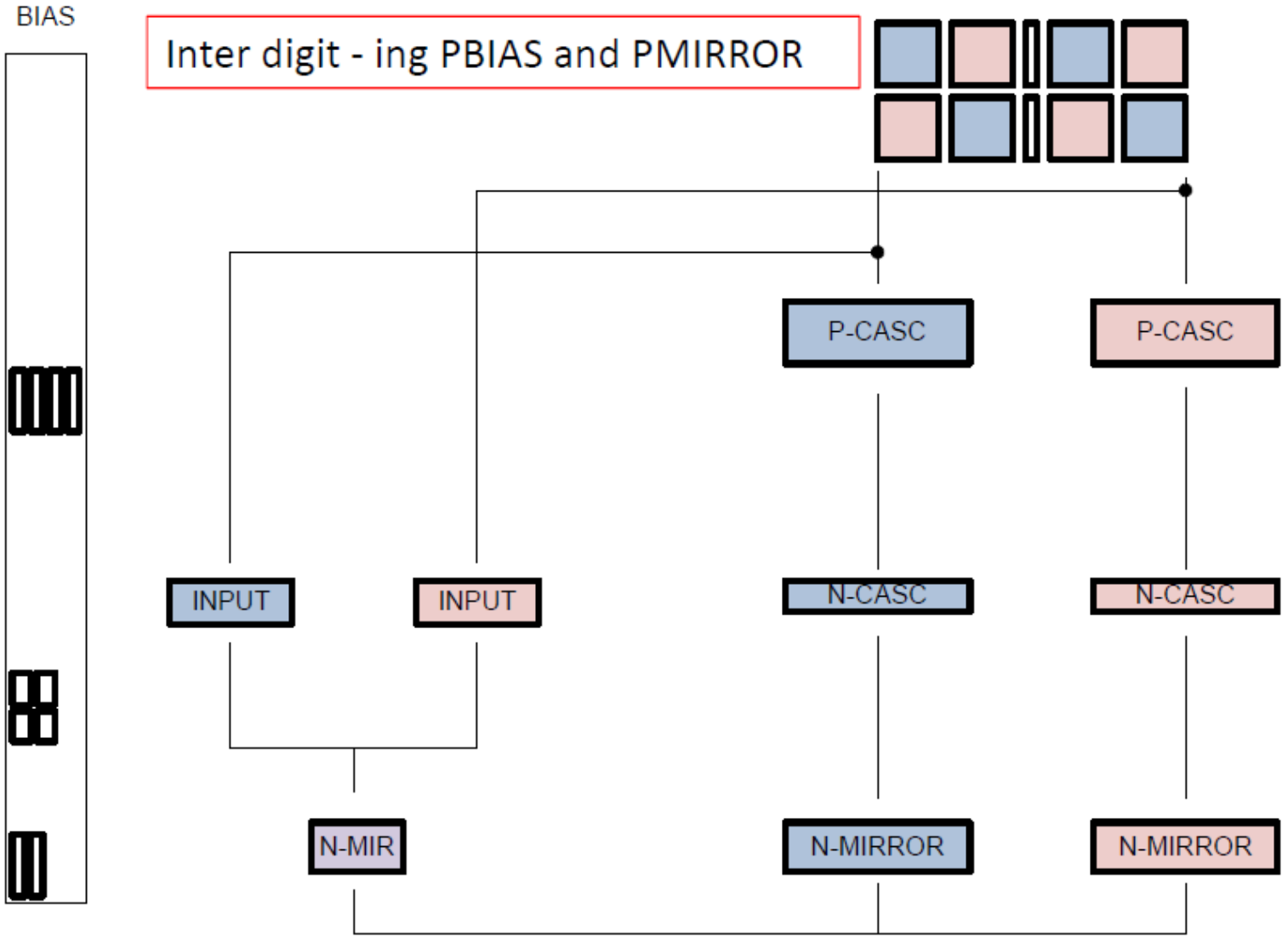
Symmetry for a Folded Cascode Amplifier



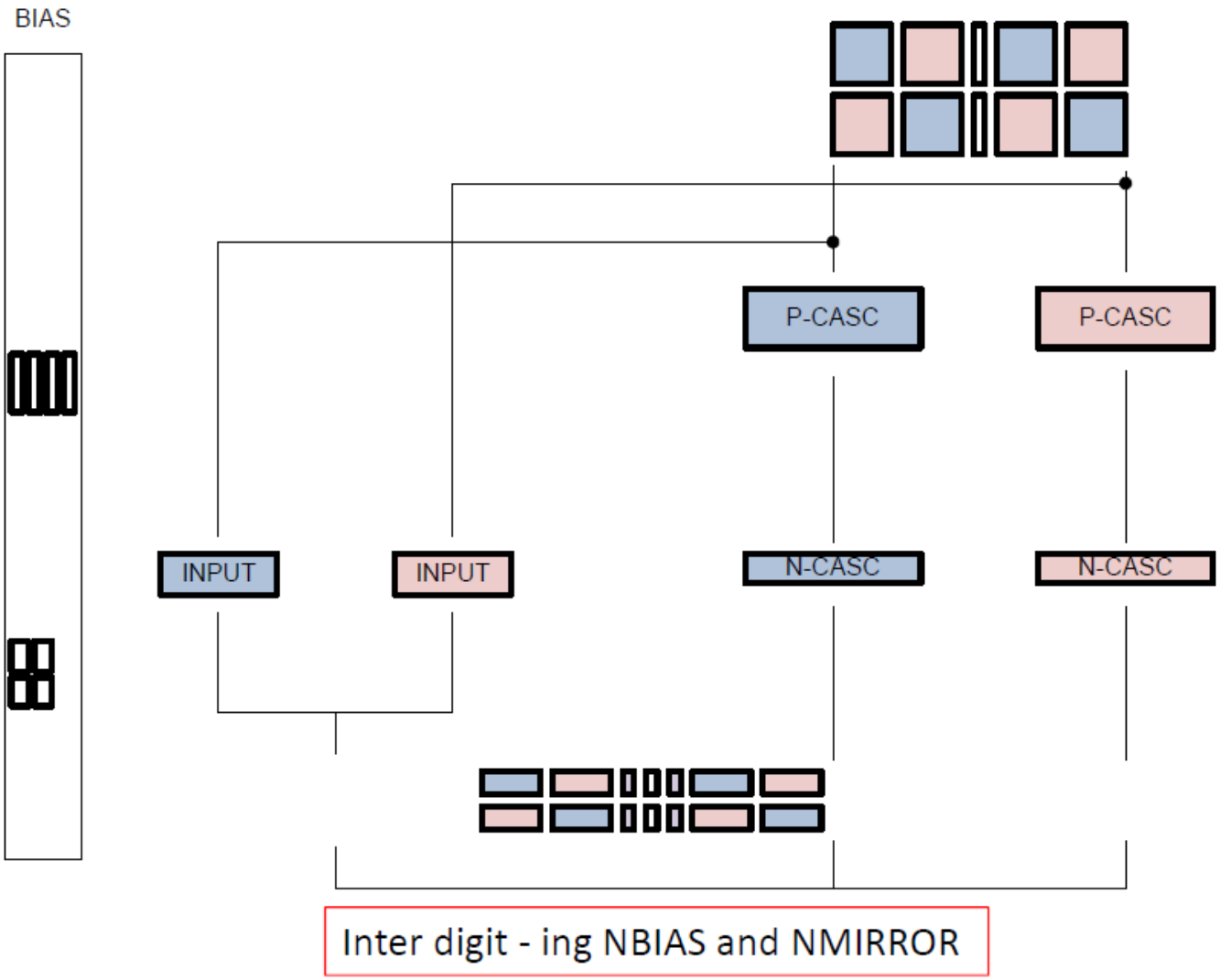
Symmetry for a Folded Cascode Amplifier



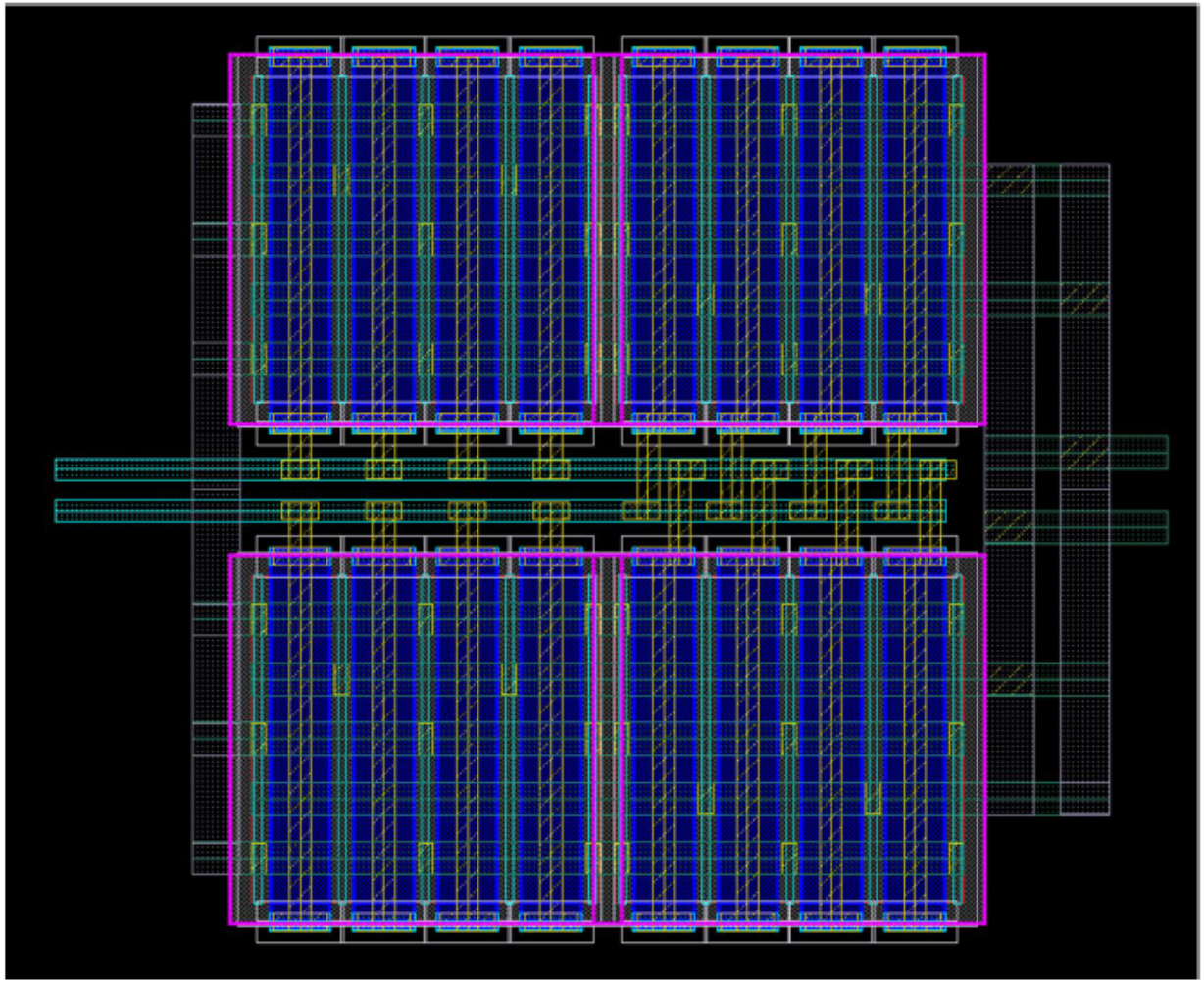
Symmetry for a Folded Cascode Amplifier



Symmetry for a Folded Cascode Amplifier



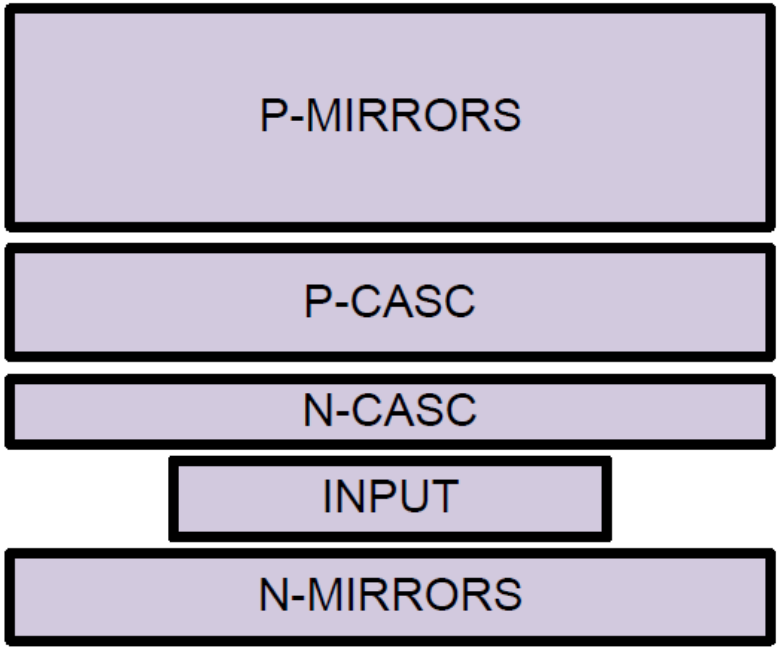
Symmetry for a Folded Cascode Amplifier



Common Centroid input pair ...

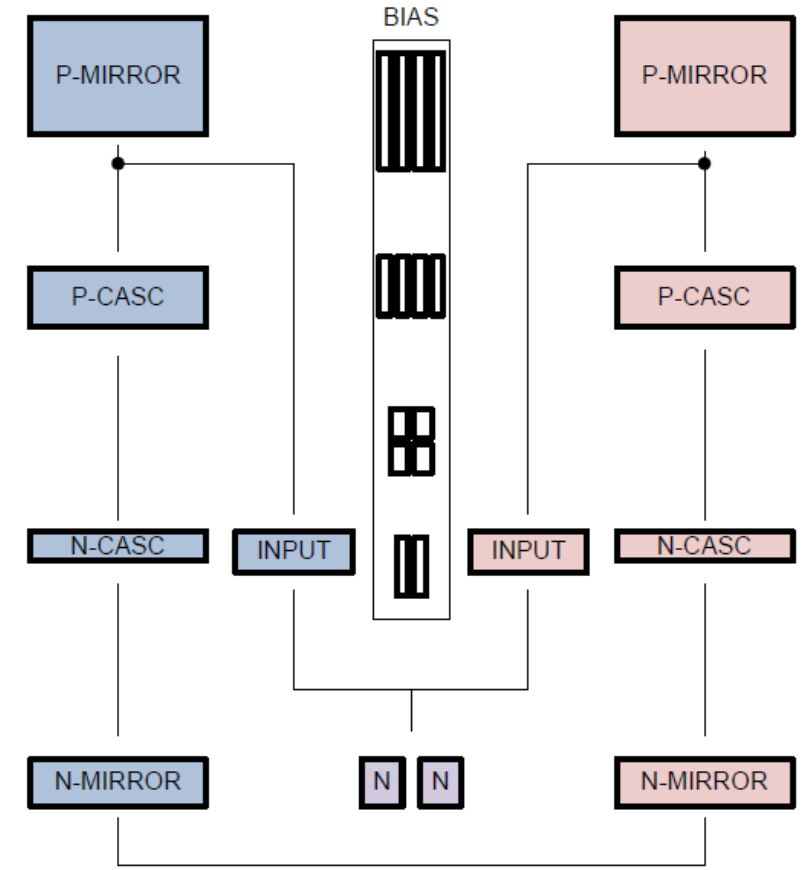
Symmetry for a Folded Cascode Amplifier

Symmetry at Transistor Final Layout



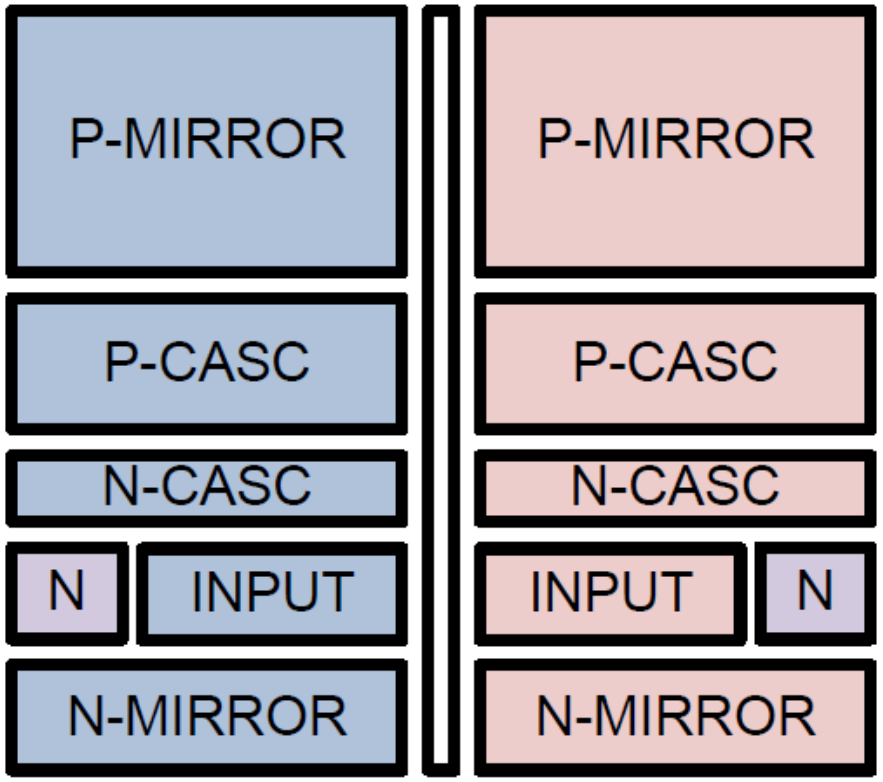
All transistors interlinked
+ Good matching
- Poor parasitics

Symmetry at Top-Level



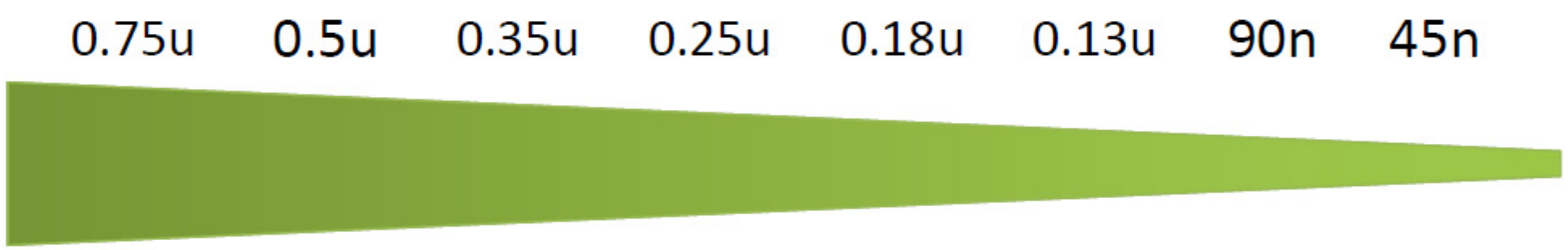
Biasing Placed in the middle of identical POS/NEG blocks

Symmetry at Top-Level

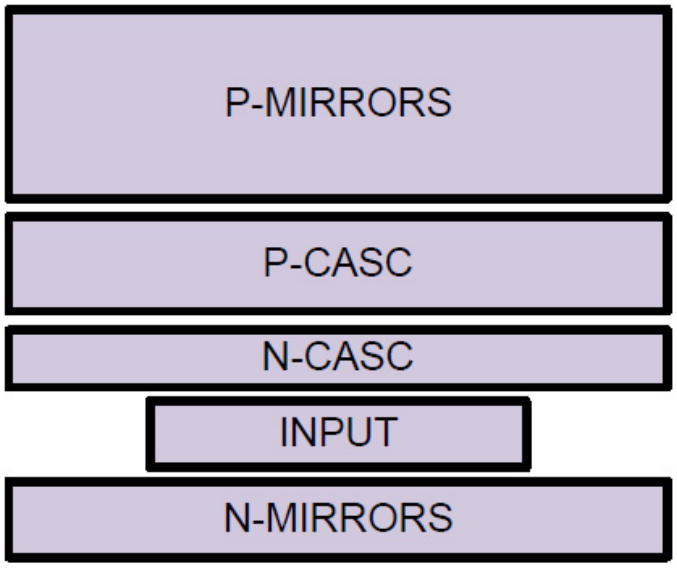


"Pseudo" differential
Mirrored Layout
+ Good parasitics
- Poor gradient matching

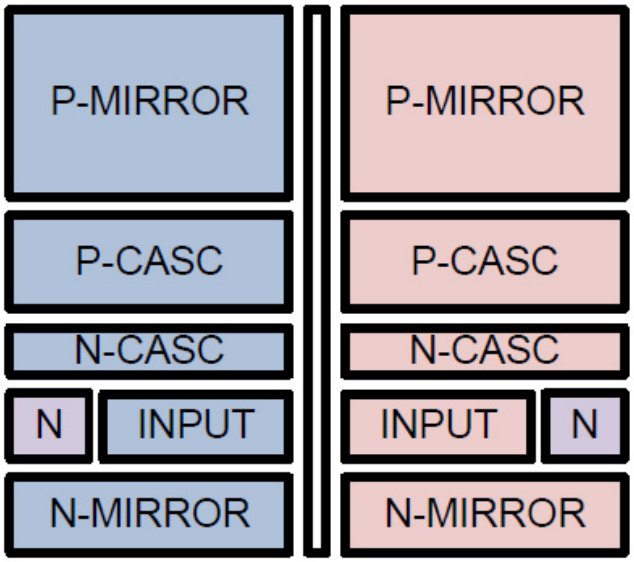
Symmetry at transistors vs. Symmetry at top level



Symmetry at Transistors



Symmetry at Top-Level



Rules for Capacitor Matching

- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections' contribution
- Don't run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices

Rules for Resistor Matching

- Use the same material
- Identical geometry, same orientation
- Close proximity
- Interdigitate arrayed resistors
- Use dummy elements
- Place resistors in low stress area
- Place resistors away from power devices
- Use shielding

Rules of Matching

- Place matched devices close to each other.
- Keep devices in the same orientation.
- Choose a middle value for your root component.
- Interdigitate.
- Surround yourself with dummies.
- Cross-quad your device pairs.
- Match the parasitics on your wiring.
- Keep everything in symmetry.
- Make differential wiring identical.
- Match device widths.
- Go large.

Computer Lab

1. A: 20um/0.5um NCH3, B: 20um/0.5um NCH3
2. A: 5pF MIM_CAP, B: 5pF MIM_CAP
3. A: 50K RNPOLYU3, B: 50K RNPOLYU3

Match A and B!

集成电路版图设计技术

Layout Techniques of the Integrated Circuit

聂凯明

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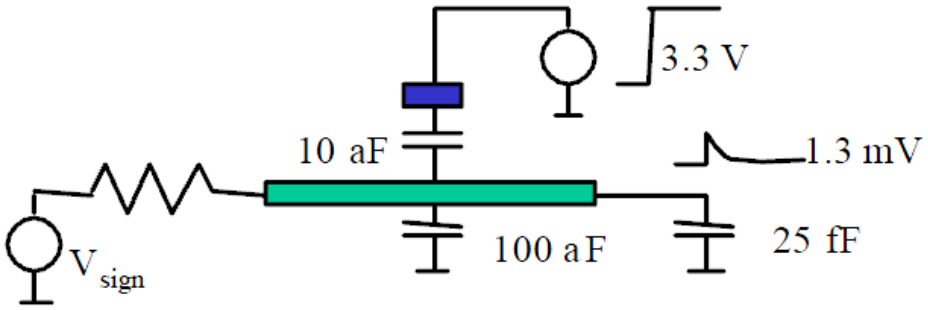
Lecture 5:

Noise

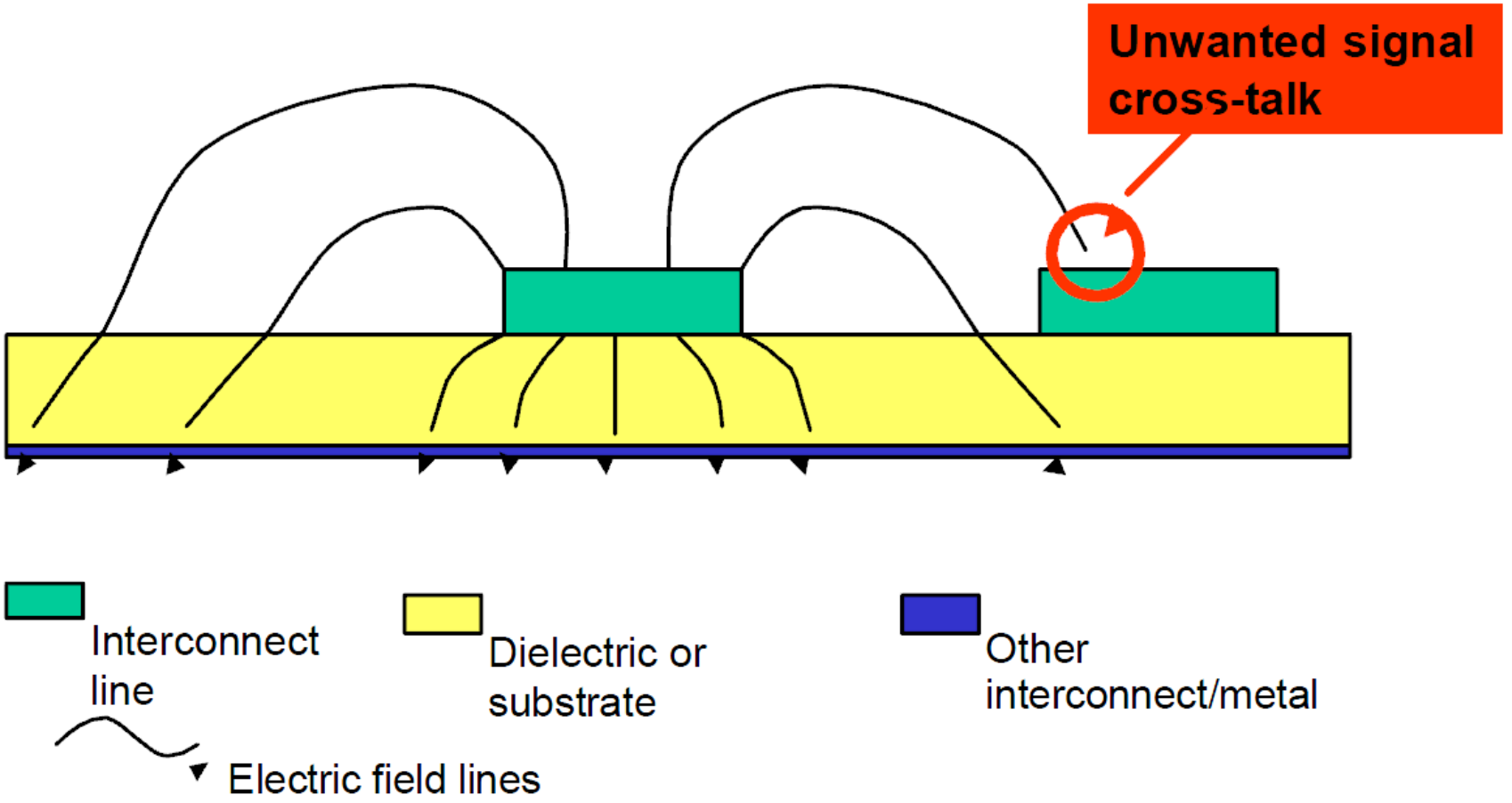
Cross-talk

- Consider the crossing of a clock line with a signal line.
  - The clock swing is 3.3 V
  - The crossing area is 0.5 μ^2
  - The signal line is 25 μ^2, the input capacitance is 0.025 pF
  - The metal-metal cap is 20 aF/μ^2 and the metal-substrate is 4 aF/μ^2
- Estimate the spur on the signal line

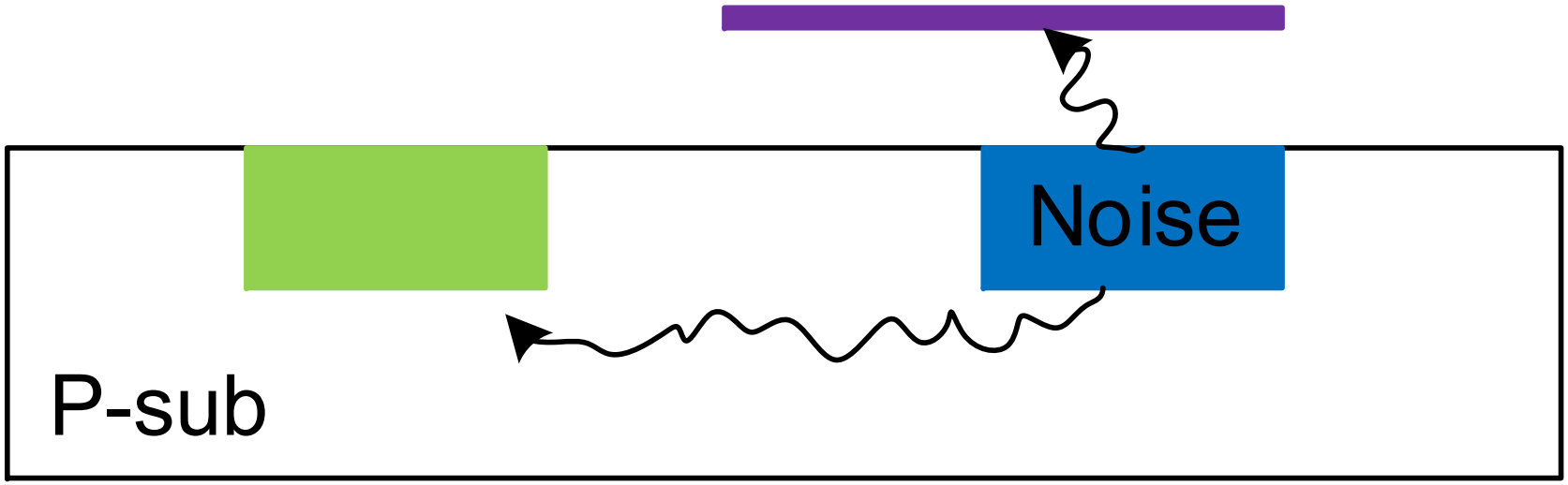


$$V_{spur} = 3.3\frac{10}{25110}$$

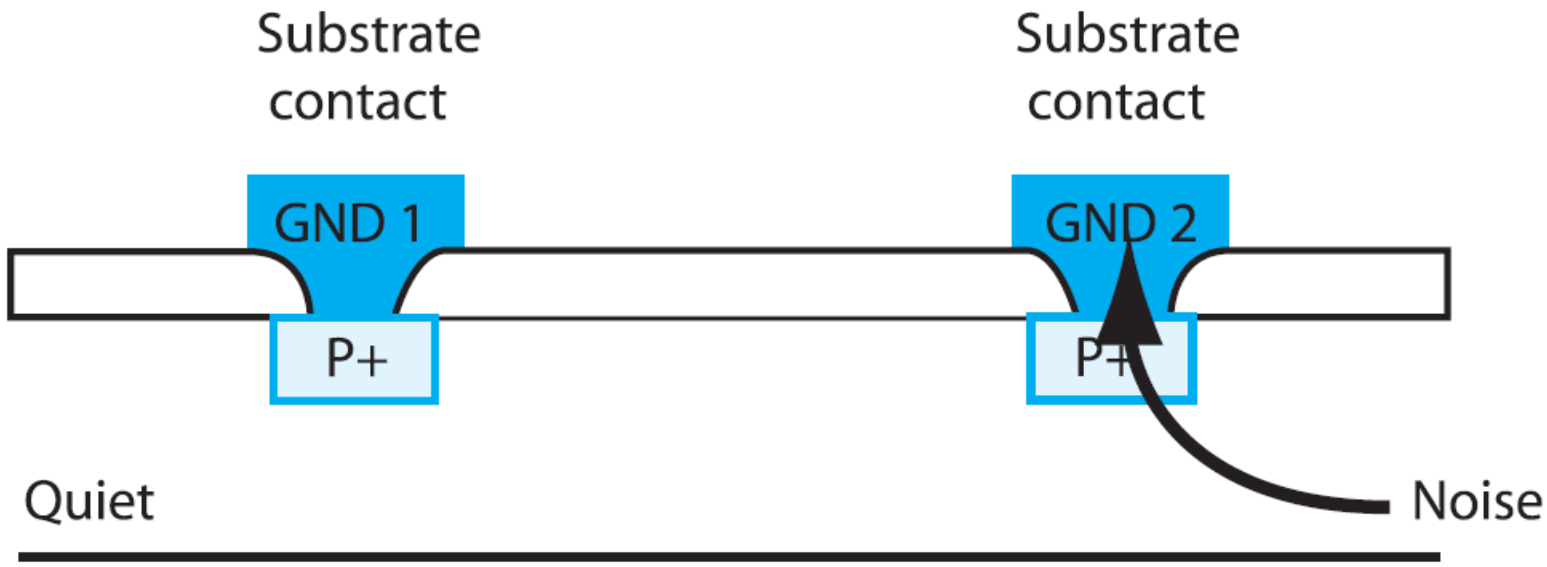
EM Field Near Traces



Substrate Noise

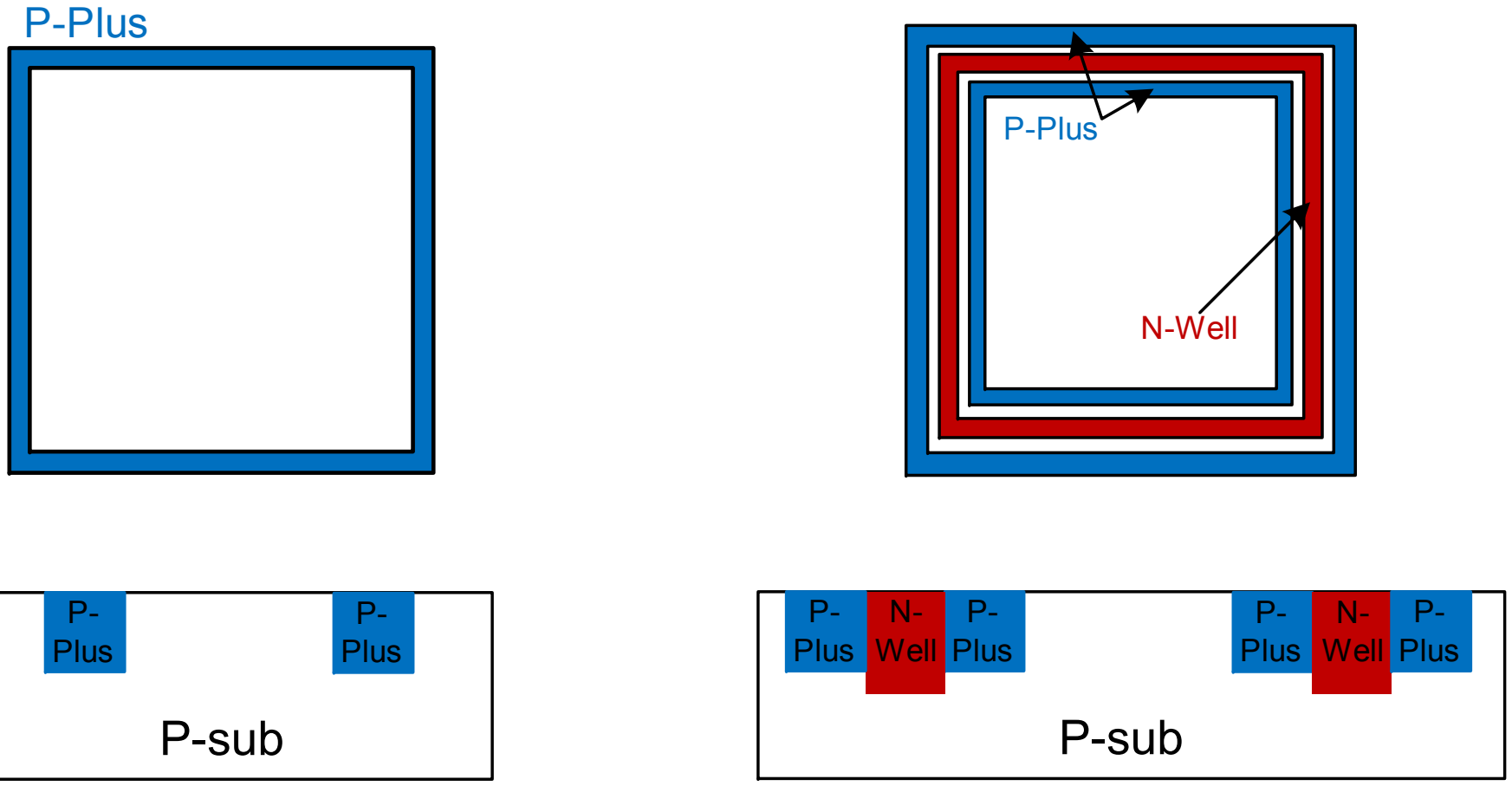


Solution: Guard ring

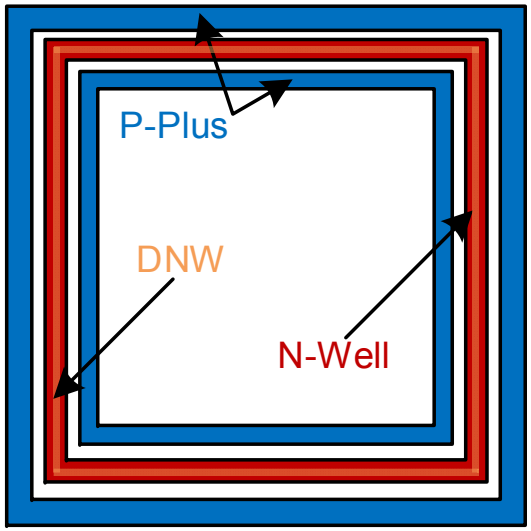


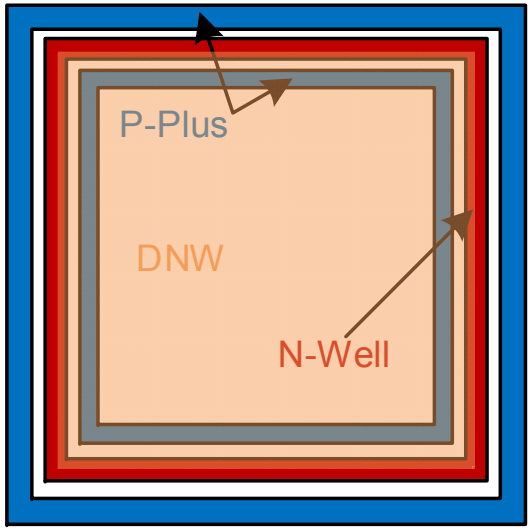
Placing some slippery exits in the way helps eliminate traveling noise.

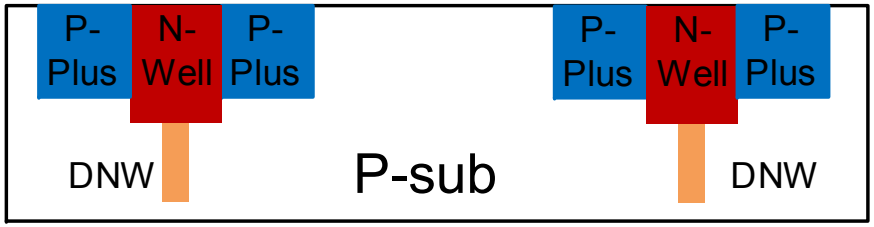
Solution: Guard ring

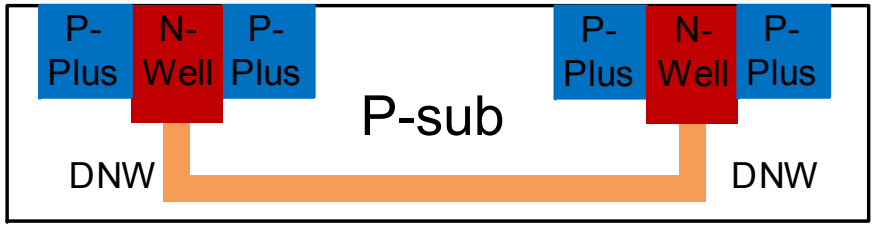


Solution: Guard ring

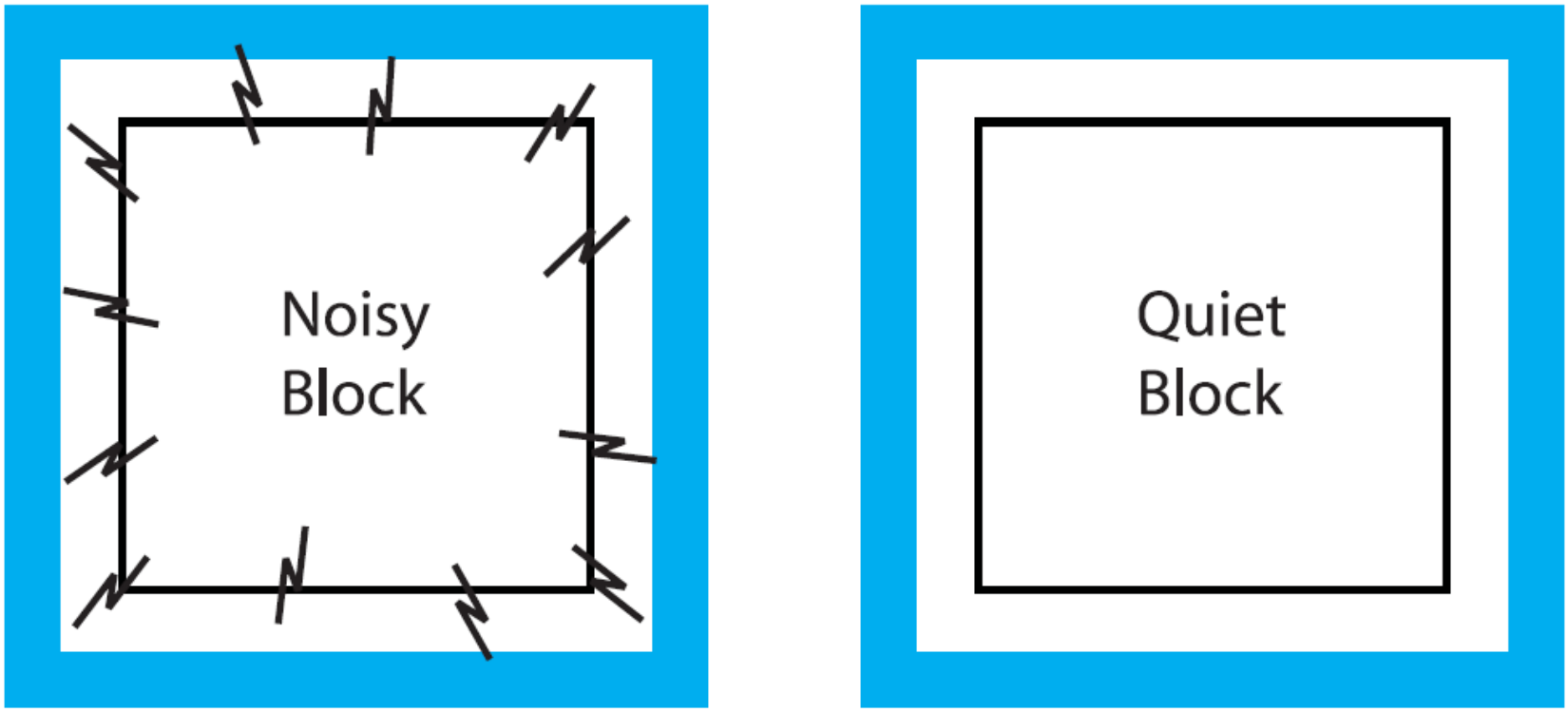




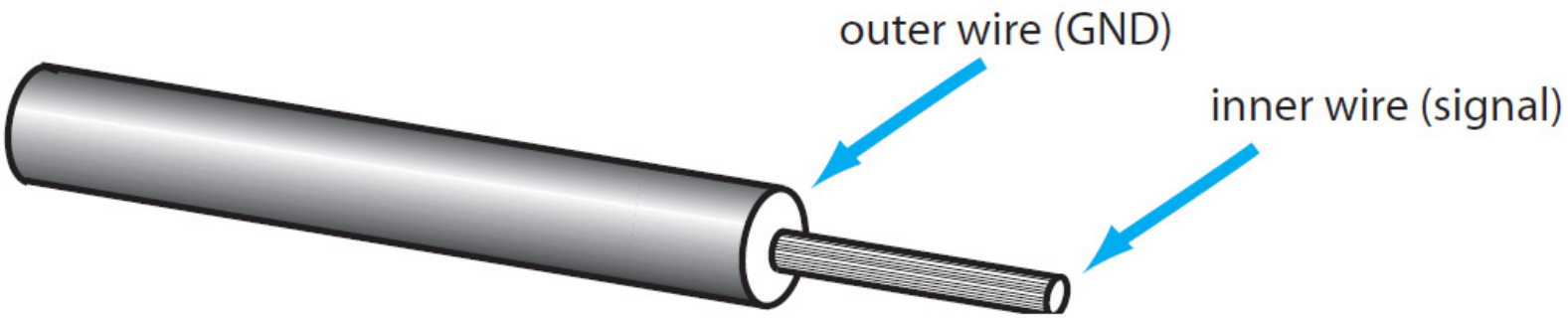




Solution: Guard ring

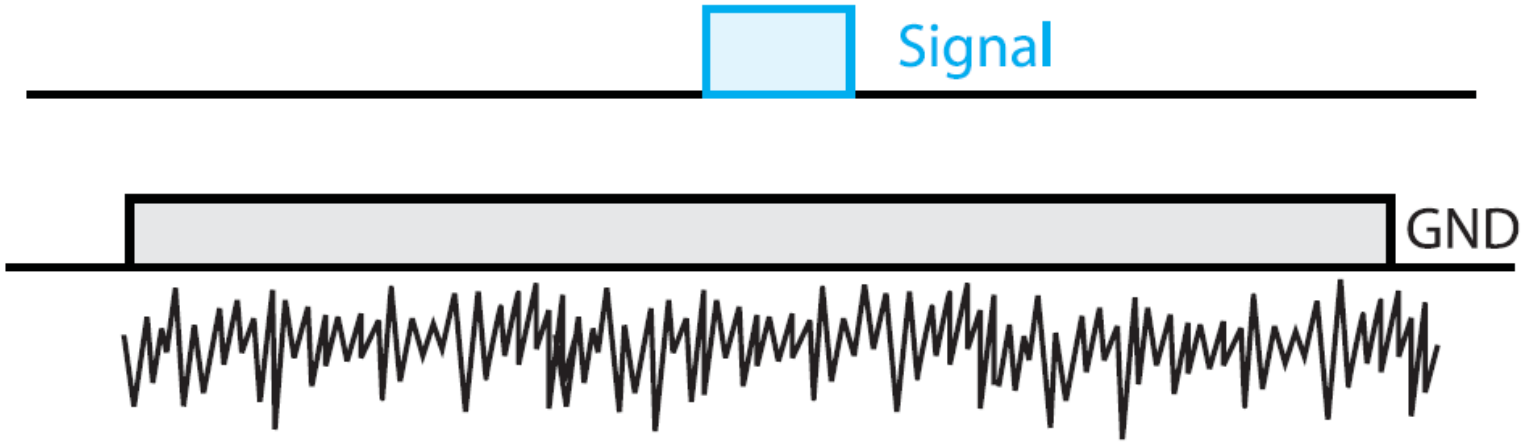


Solution: Coaxial Shielding



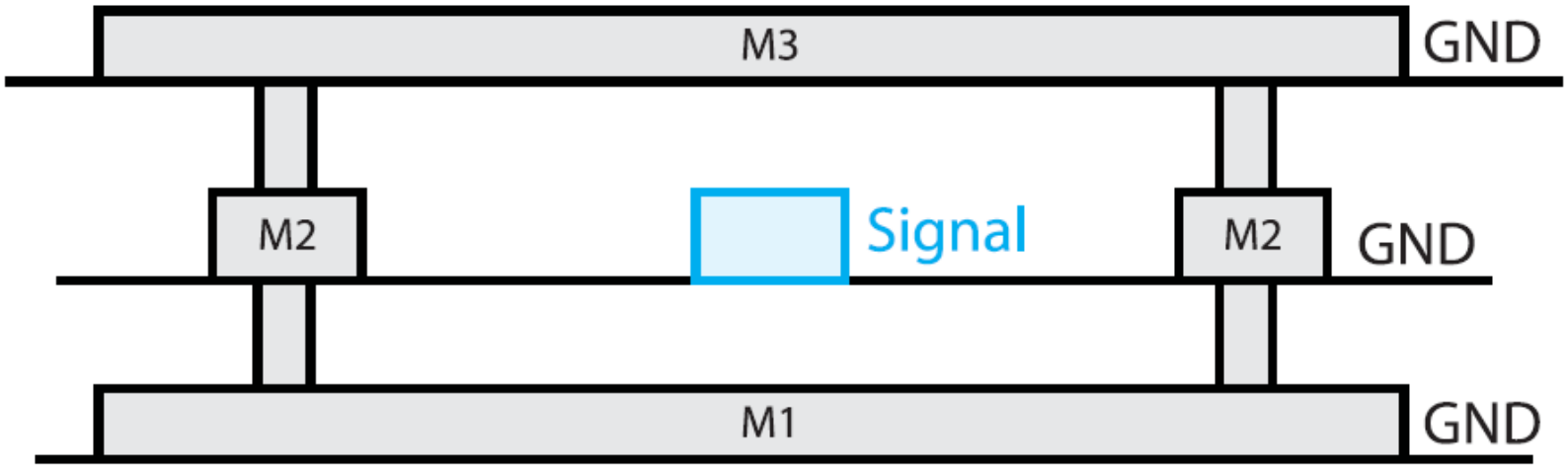
Coaxial cable (coax) comes with built-in shielding all around the signal wire.

Solution: Coaxial Shielding



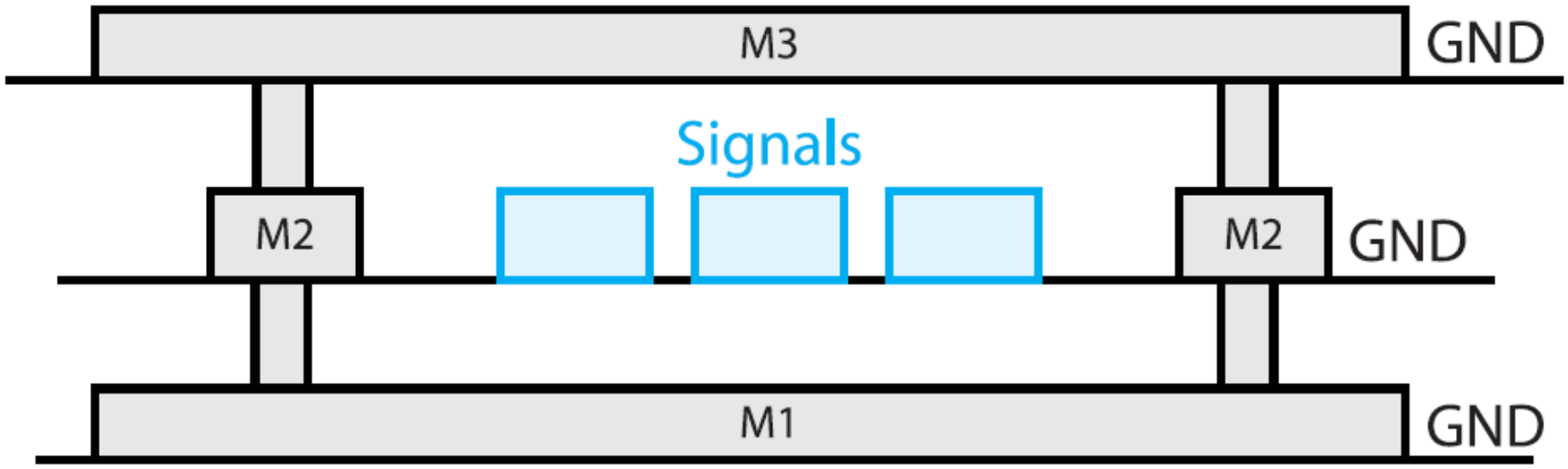
Shielding the signal using Metal One.

Solution: Coaxial Shielding



Surrounded by shielding.

Solution: Coaxial Shielding

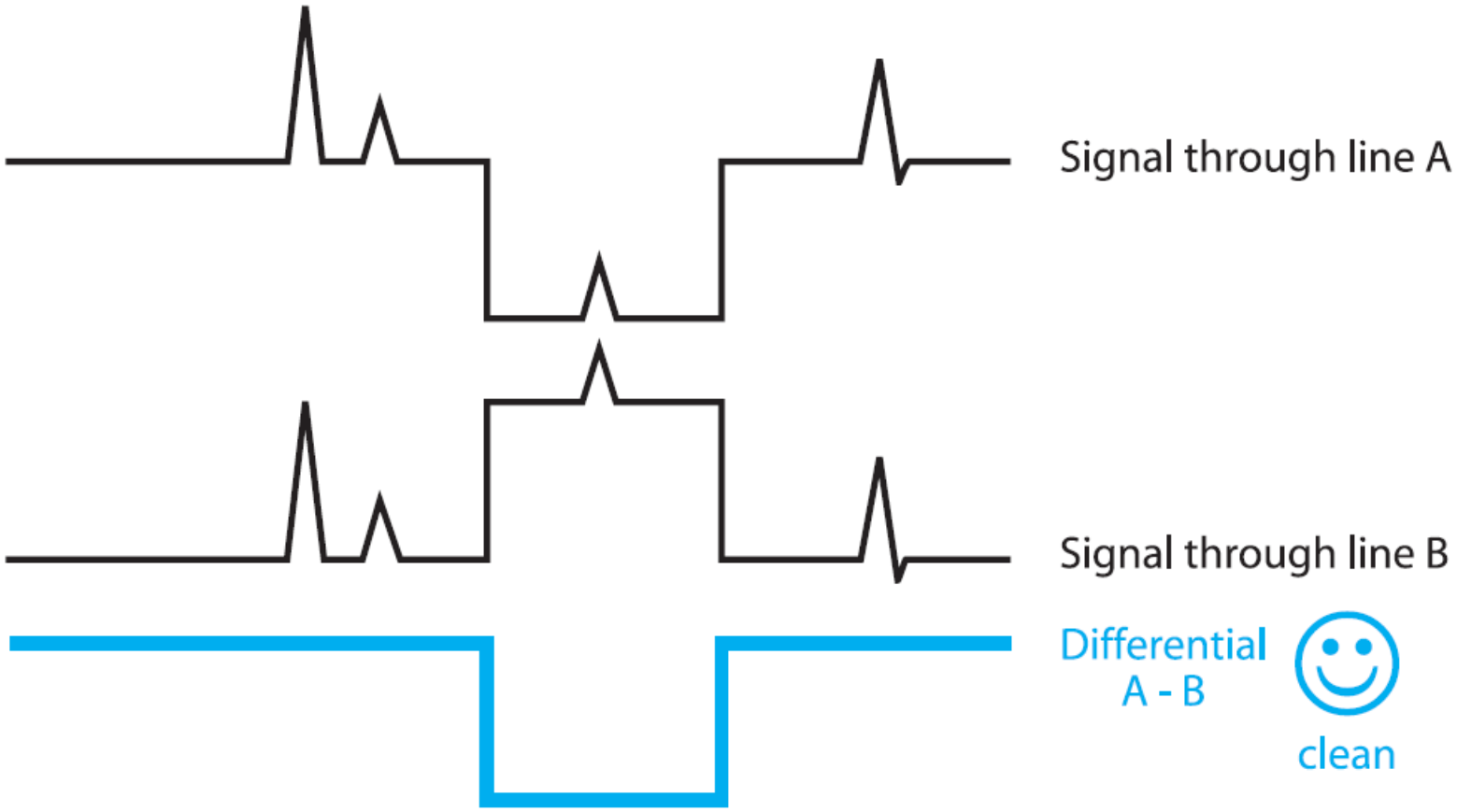


Great place for shielding lots of quiet signals, or lots of noisy signals, from the outside world.by shielding.

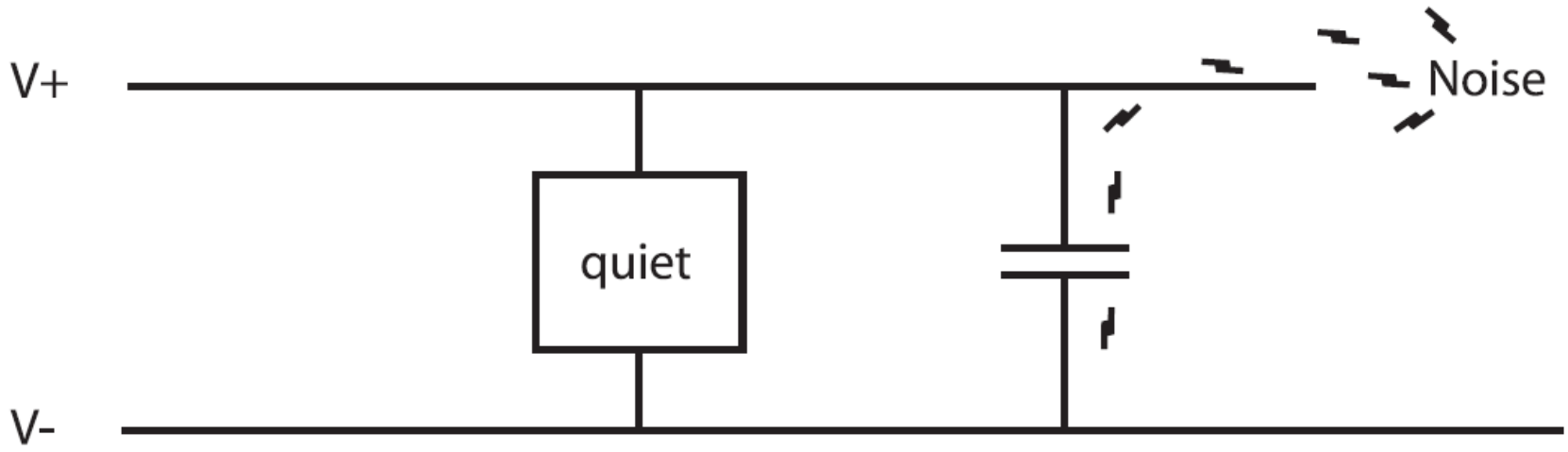
Solution: Coaxial Shielding

N-Well also can be used for shielding the noise from substrate.

Solution: Differential Signals

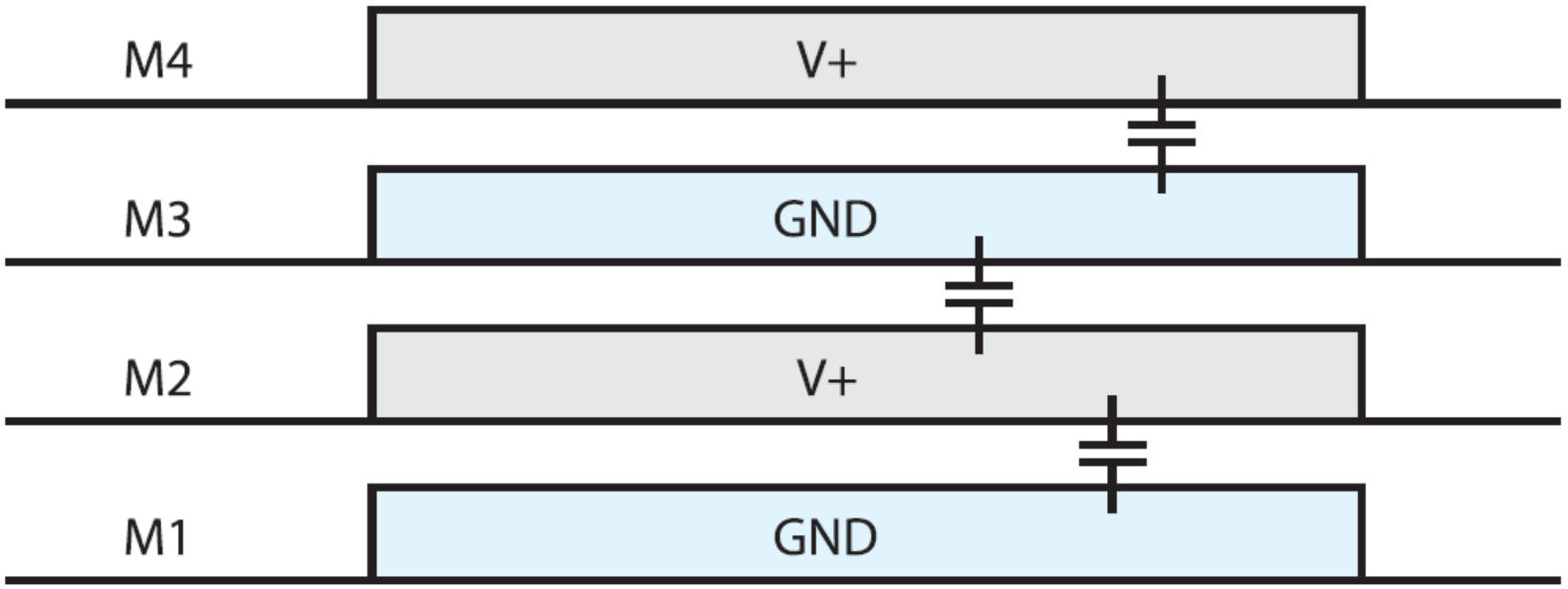


Solution: Decoupled Power Rails



Traveling down the capacitor to ground is much easier for a high frequency noise signal than trying to charge onward through the circuitry.

Solution: Decoupled Power Rails



Small capacitances form for free, if you stack your power rails.

Computer Lab

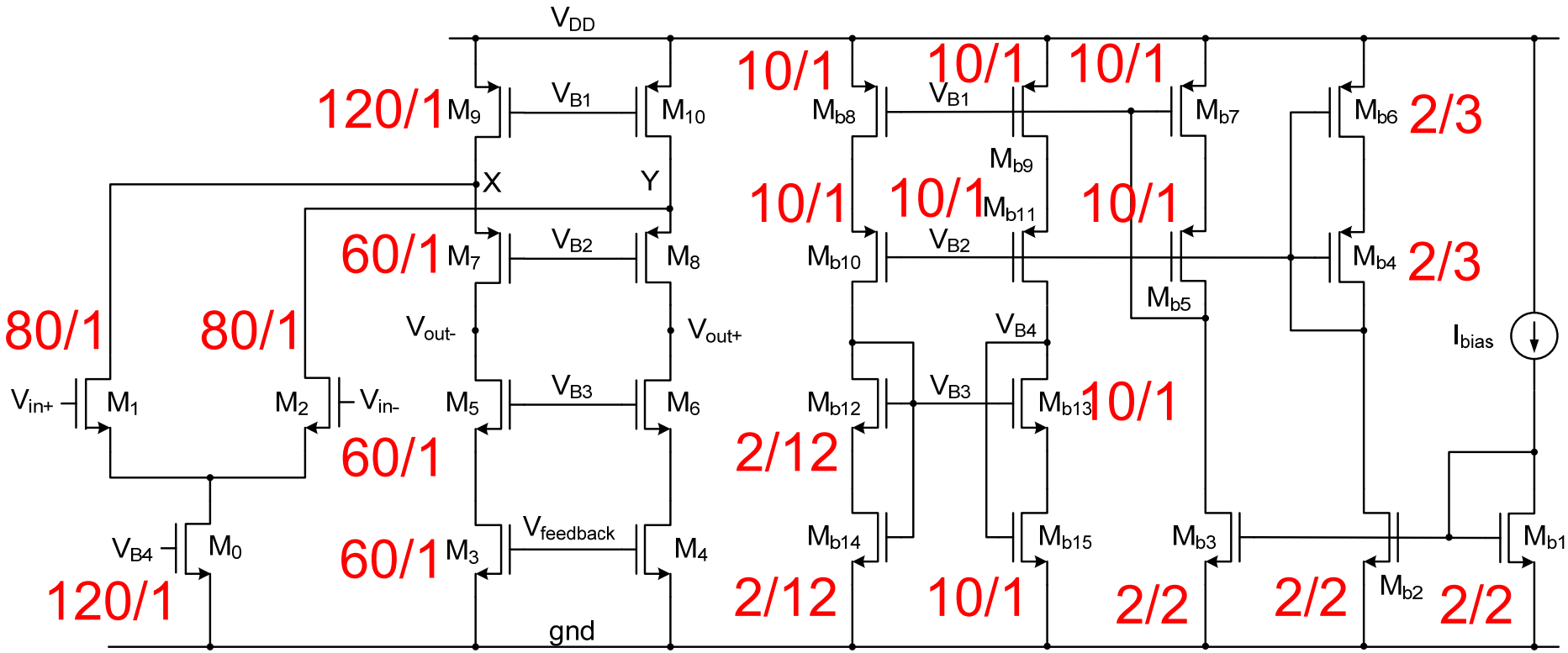
1. Draw a PNP guard ring with deep N-well.

2. Draw a coaxial shielding for a M2 wire.

3. Complete the layout design of the OPA shown in the next page, and protect it with a PNP guard ring.

Computer Lab

Unit: um



集成电路版图设计技术

Layout Techniques of the Integrated Circuit

聂凯明

天津大学专用集成电路设计中心

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Lecture 6:

Floorplan and ESD

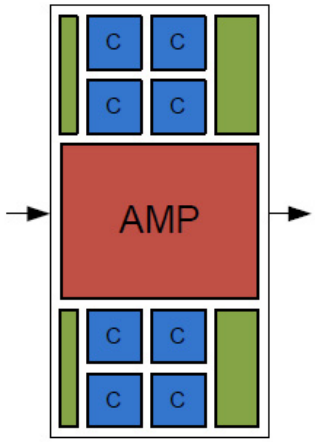
Block floorplan

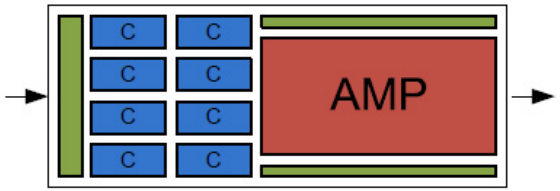
- Signal flow
  - Need to consider the routing around the sub block
    - E.g. feedback network
    - Minimise input-output and stage-stage crosstalk, particularly around blocks with high gain or delay
  - What to do across the block (Eg Analog, digital, references)
    - Where do the signals arrive, where does it leave?
    - Don't create a problem for someone else to solve
- Power supplies
  - What is the global strategy and what metal layers will be used?
- Wells
  - Organization, well spacing and overlap is the largest design rule
  - Deep Nwell, not always compatible with sub-blocks,
    - strategy to use deep nwell needs to be decided early on

Block floorplan

Building up a macro-block
Example Pipelined ADC

Within one stage of the pipelined ADC, the amplifier, the capacitors and the other circuitry can be arranged in different ways.





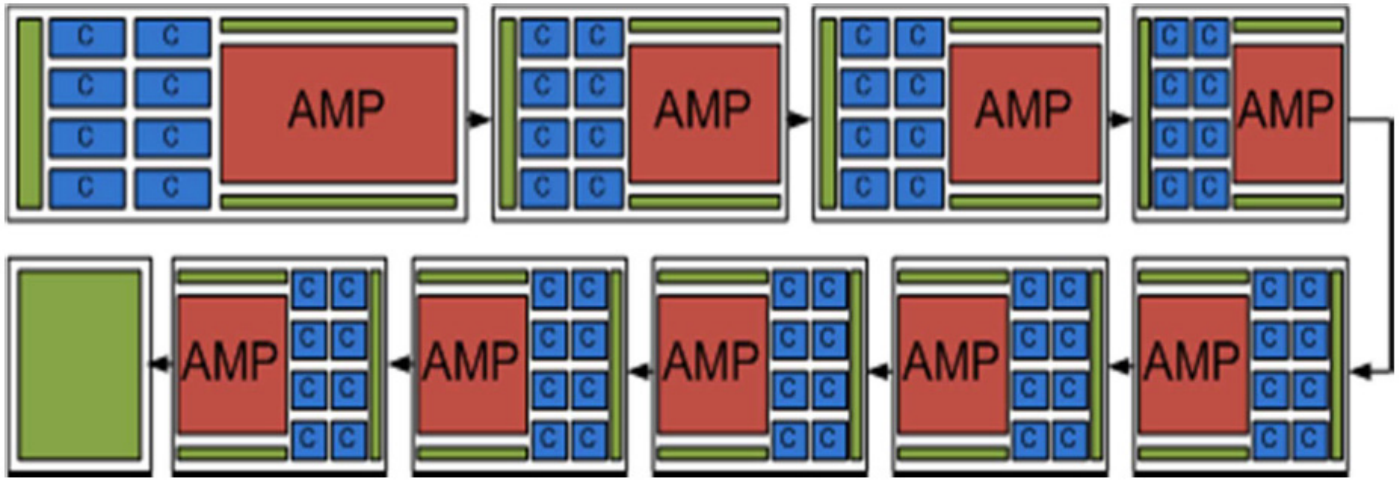
Things to consider within the Stage:

- Compactness of Stage Layout
- Critical Signal routing inside the stage
- Effect of Parasitic

Block floorplan

Example (1) 12bit pipeline ADC Floorplan

The 'U' Shape



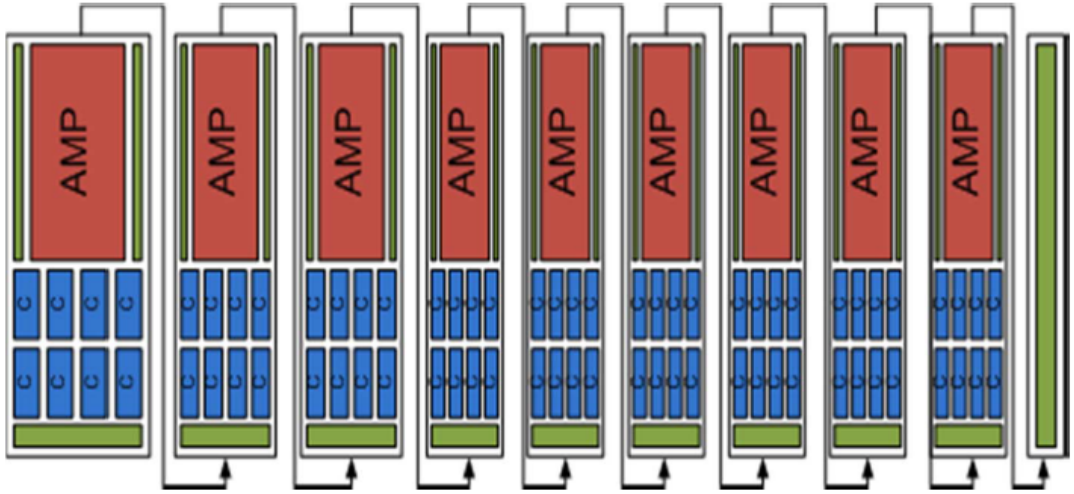
+ Results in simple layout of each stage
+ It can be easier to scale the stages

- The low res stages are close to the front end
- Distribution of the clock can be difficult

Block floorplan

Example (2) 12bit pipeline ADC Floorplan

The 'up-down' floorplan



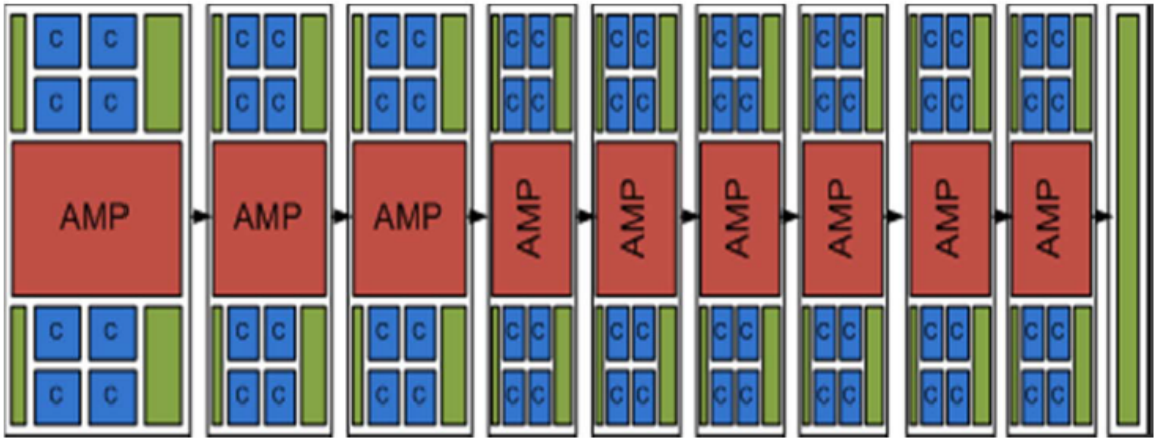
+ Distribution of clock is simple
+ Uniformity between the stages can be maintained
+ High-Res is far away from Low-Res

- Scaling of stages is difficult
- It's difficult to balance the routing between Pos and Neg in a differential system
- In practice managing unwanted parasitic can be difficult

Block floorplan

Example (3) 12bit pipeline ADC Floorplan

The 'left-right' floorplan



+ Distribution of clock is simple
+ Uniformity between the stages can be maintained
+ High-Res is far away from Low-Res
+ cross stage parasitic are minimized

- Internal routing and layout of each stage can be very difficult
- Scaling of stages for power can require major rework.

Block floorplan

Clock phases
Switches

Capacitor array

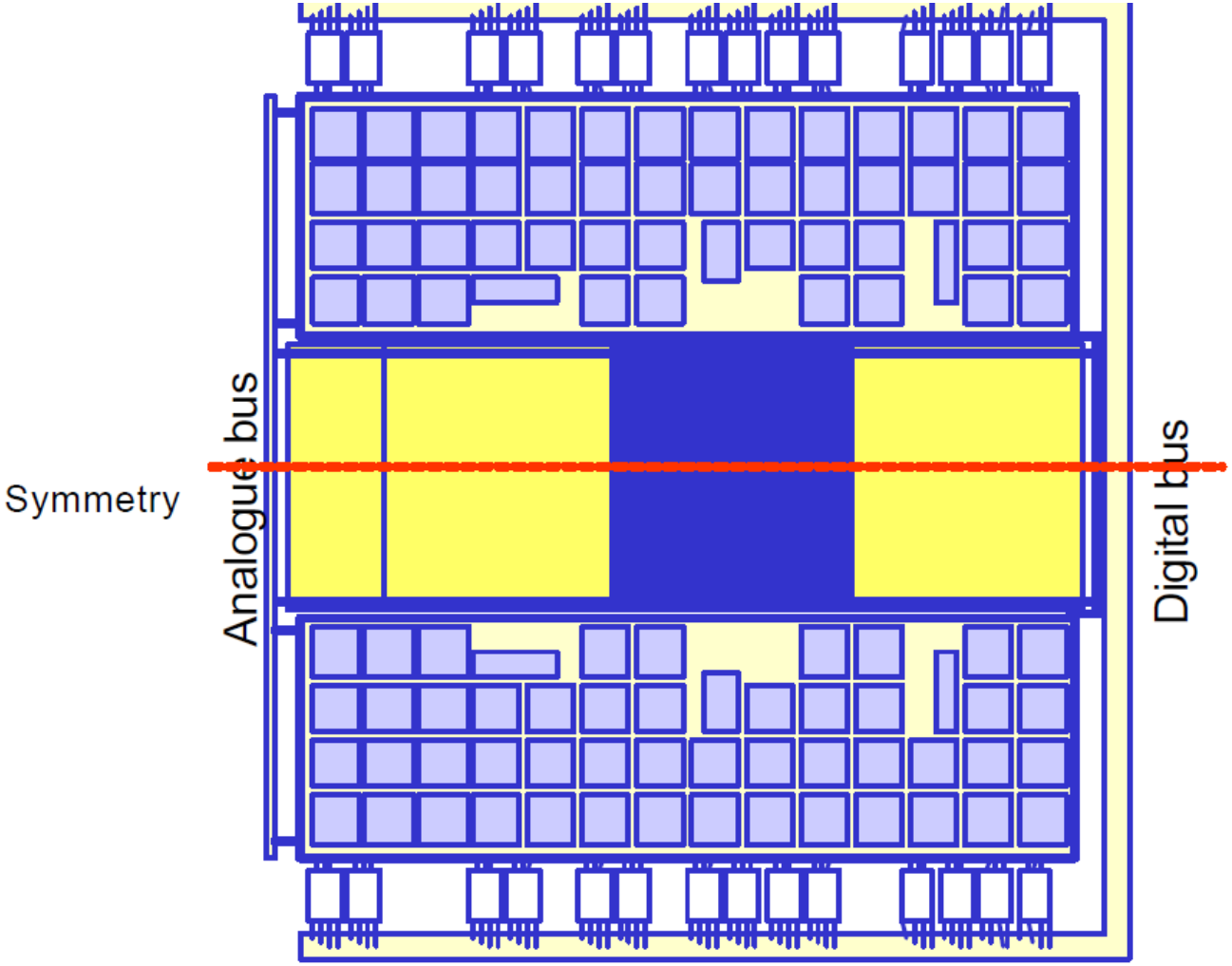
Analog bus

Analog cells

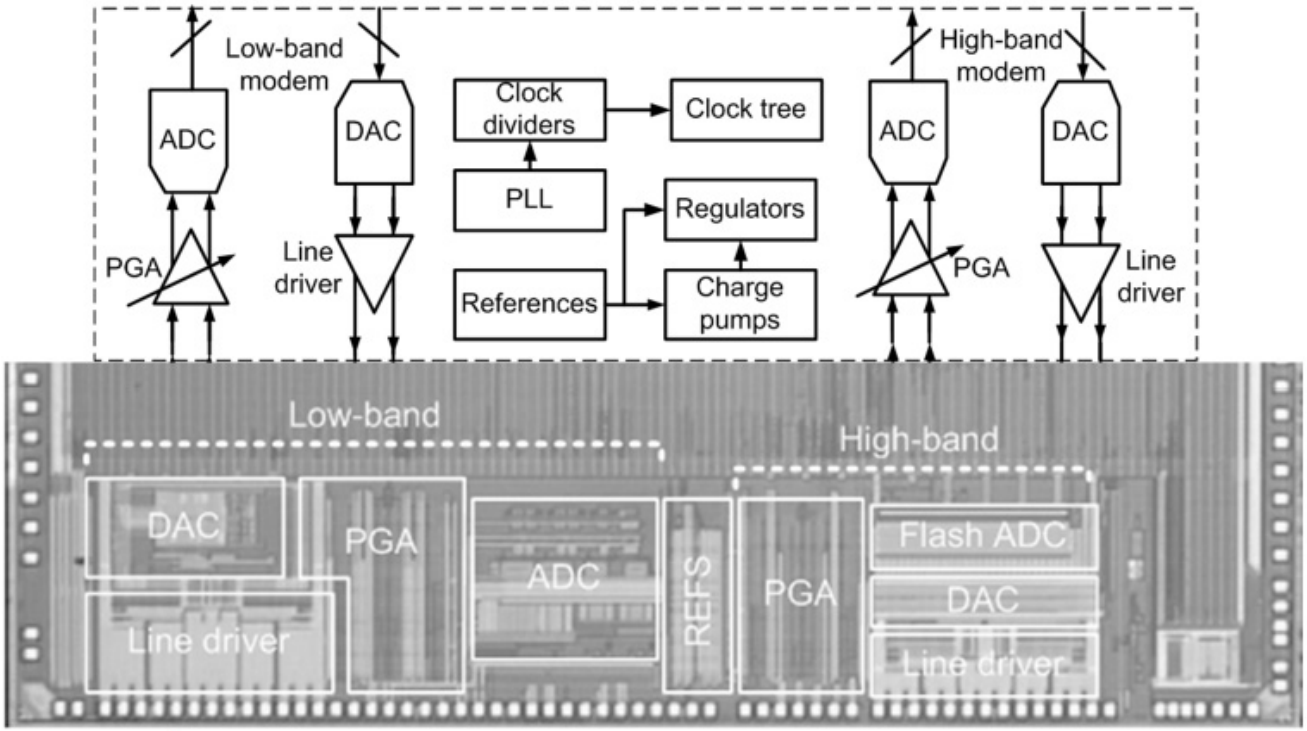
Analog bus

Capacitor array

Switches
Clock phases



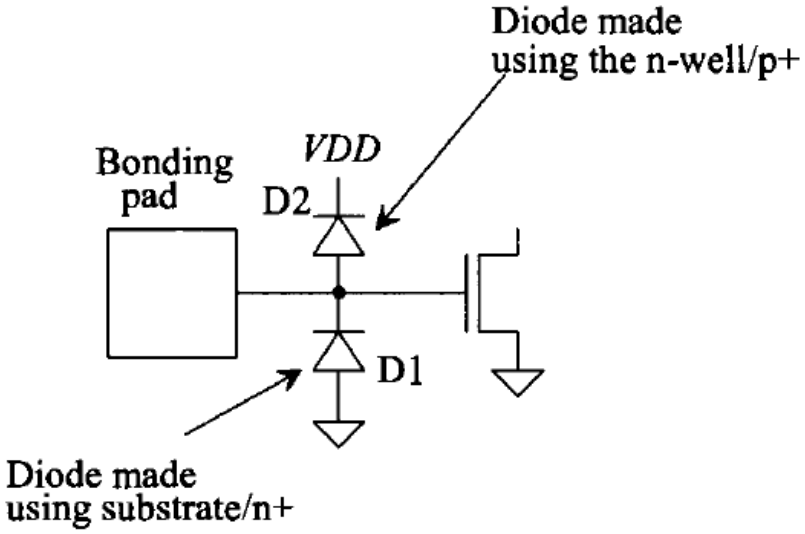
Block floorplan

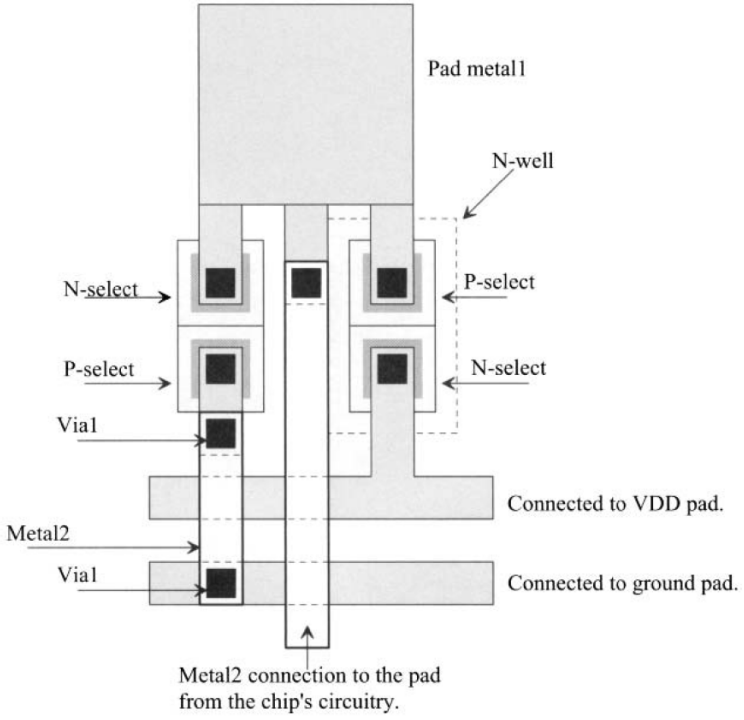


- Need to consider
  - Separation of functions (e.g. RX/TX or bands)
  - Alignment to pins/pads
  - Power routing
  - Reference routing
  - Clock routing
  - Form factor
  - Signal flow
  - Proximity effects
  - Crosstalk
  - Gradient effects
  - Stress effects

Electrostatic Discharge(ESD) Protection

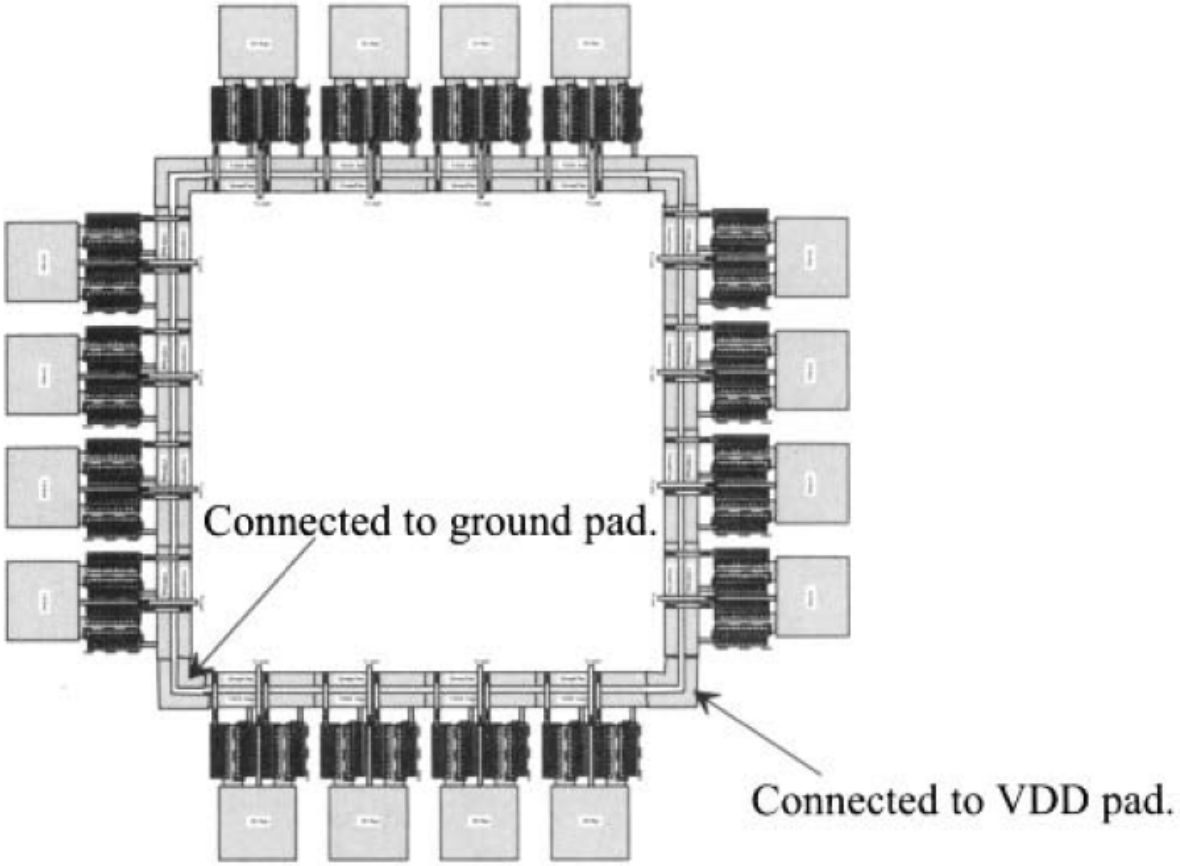
Walking across the floor, for example, causes the buildup of charge on the human body. Touching a conducting object can result in a transfer of charge or static “shock”. If the transfer of this charge is through the thin gate oxide of a MOSFET, it is likely that the gate will be damaged.





Electrostatic Discharge(ESD) Protection

Layout of a padframe using pads with ESD diodes.



Computer Lab

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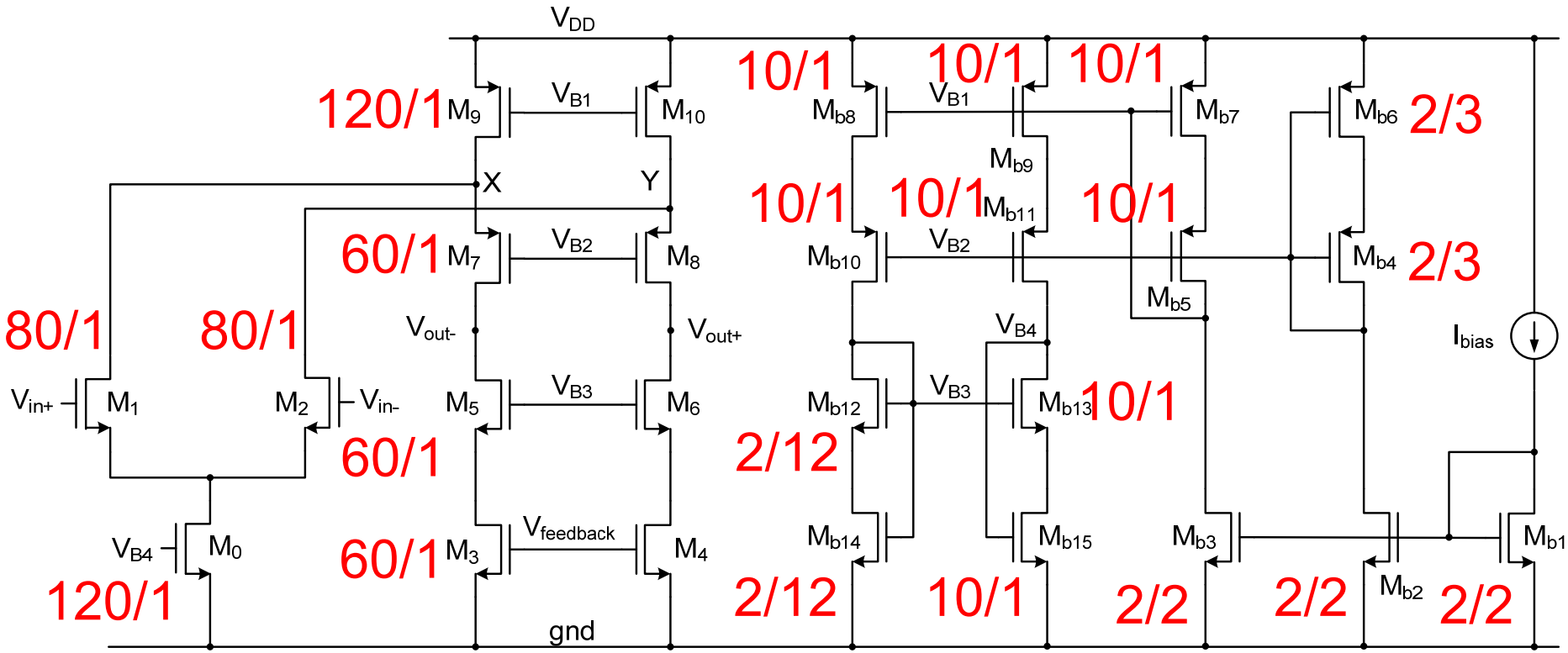

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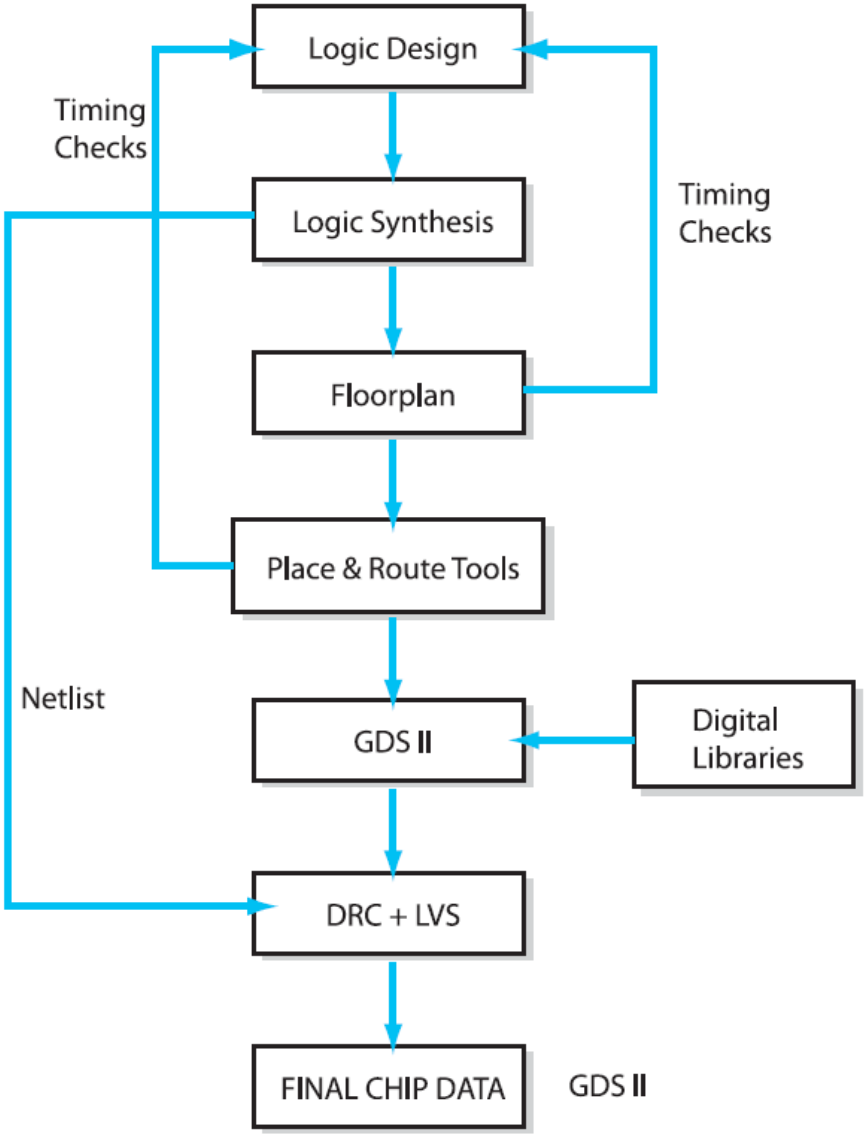
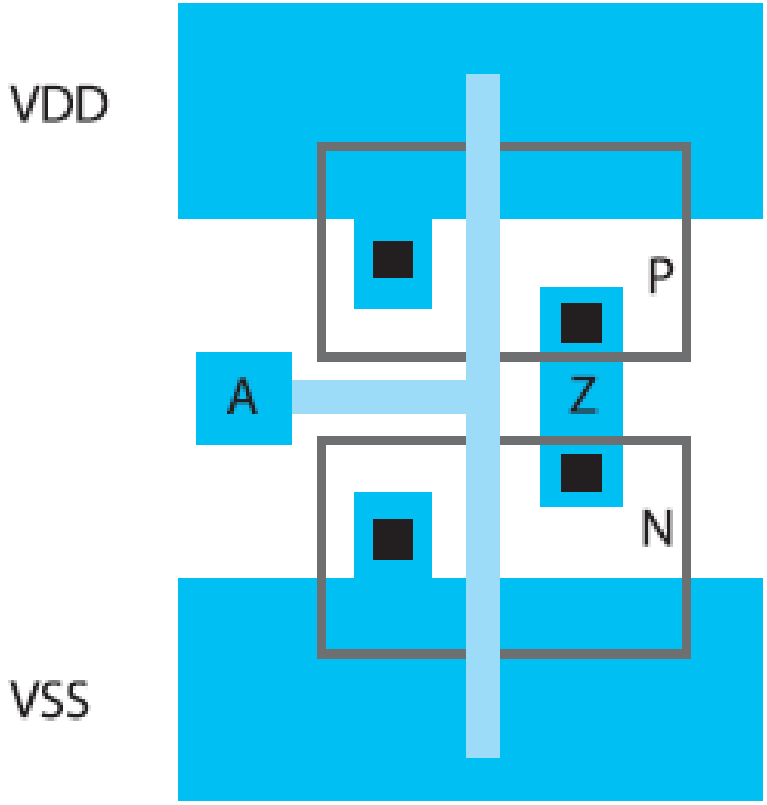
Lecture 7:

Digital Layout

Flowchart of Digital Layout Process

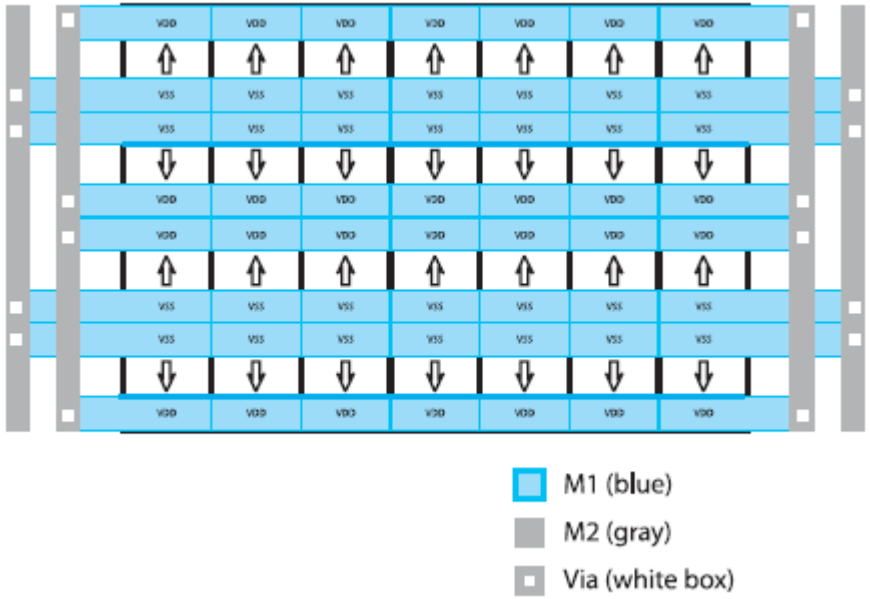


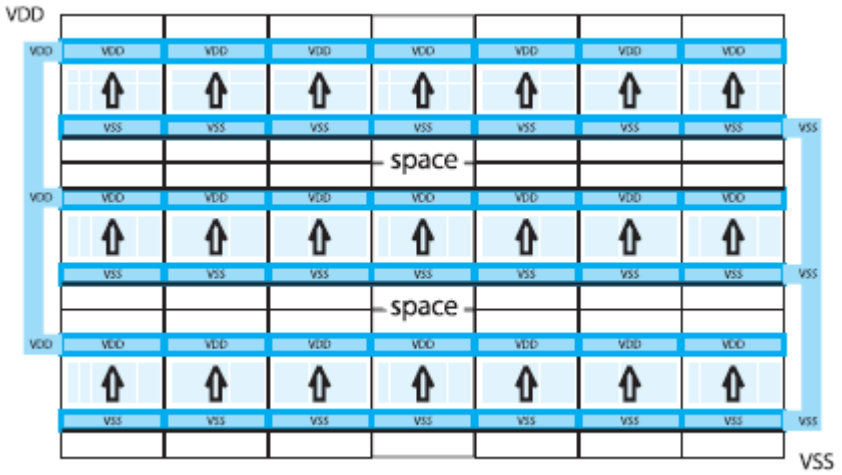
Standard Cell



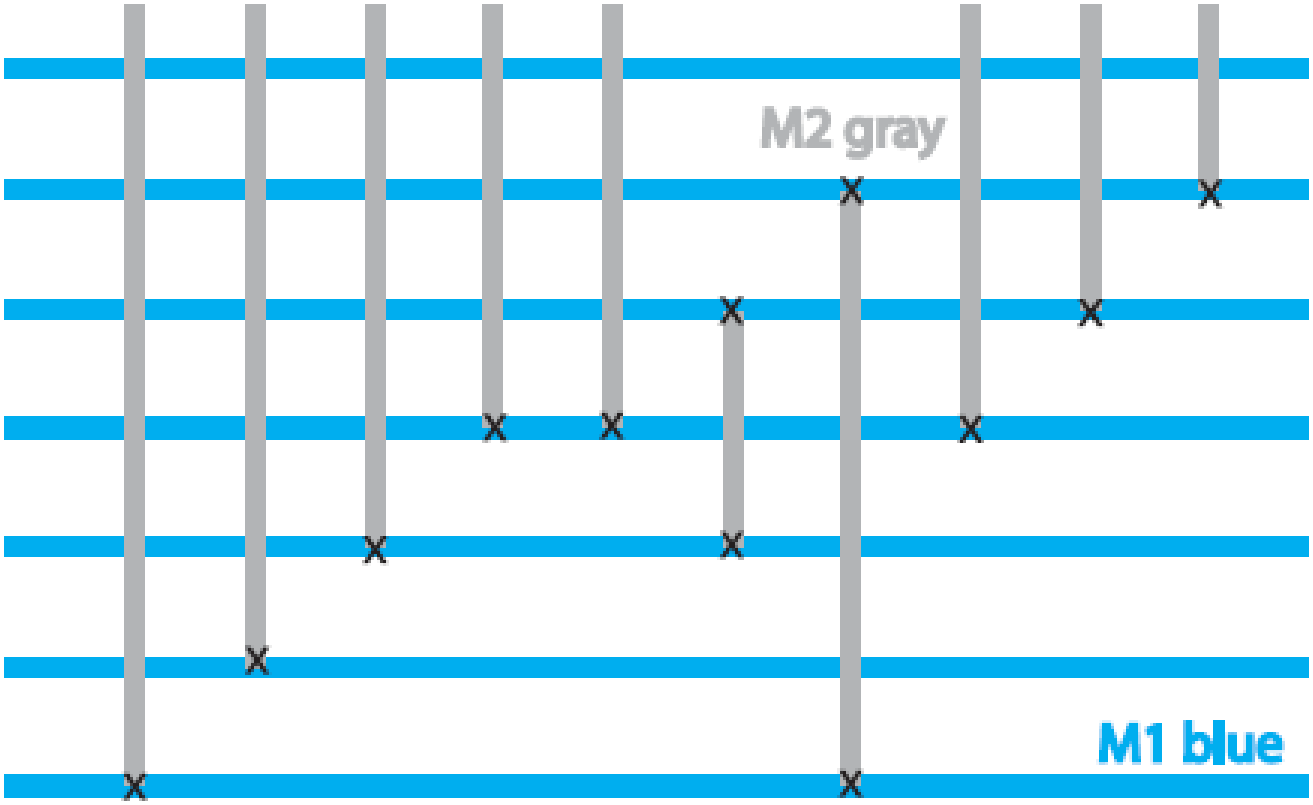
All the layouts of the logic units are optimized for consuming the minimized area, and all of them have the same height.

Floorplan

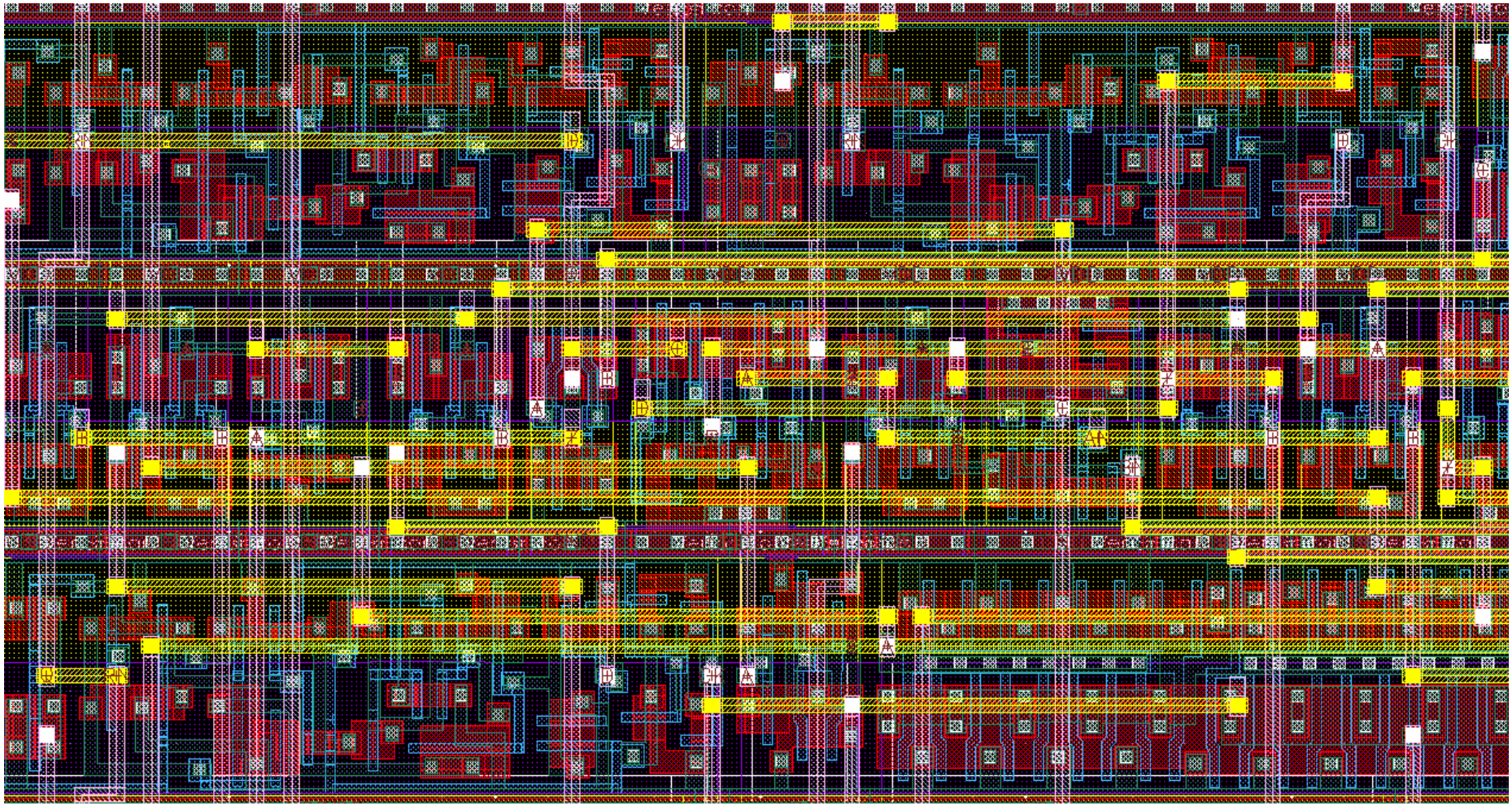




Routing



Example



Computer Lab

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